

BUFFER STORE for GIER

BS 100/2 (Elco Connectors)

Modified for DFA 200/1

LOG LIST

UNIT BUFFER MODEL BS.100/2. NO 6123

This LOG LIST contains information on modifications of the basic unit, due to Options, Engineering Change Notes, and Field Change Orders.

Do not forget to list all future modifications on this page.

OPTION ECN or FCO No.	DATE of Installation	SIGN	SHORT DESCRIPTION

A TECHNICAL DESCRIPTION
OF THE BUFFER SYSTEM

REGNECENTRALEN
FEBRUARY 1965

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SECTION 1 -- THE BUFFER SYSTEM

The Buffer System (BS) contains a 4096 word ferrite core store which may be used as a supplement to the primary core store in GIER (CS) or as a buffer between CS and up to four peripheral devices (PD) such as magnetic tape stations.

Transfers take place 42 bits in parallel and are controlled by a Priority System which allocates the transfers of waiting units one word at a time in a wired sequence so that the fastest unit can complete its transfer first. (Transfers to and from CS are always allocated lowest priority since the timing considerations of these transfers are uncritical whereas transfers between the Buffer and PDs, magnetic tape stations for instance, cannot always be interrupted). The Priority System controls five Transfer Channels (one for CS and four for the PDs), which for practical purposes work simultaneously.

Addressing of the Buffer is controlled from AD:0-11 while AD:00 indicates the direction of transfer. AD:00-11 receives its contents from one of the five registers BAO - BA4, each of which corresponds to a Transfer Channel.

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NOTICE

Regnecentralen reserves the right to alter this description and/or the equipment it describes whenever, in its judgment, such alterations are required. All persons expected to be affected by any such alterations will be duly notified.

1.

PDs are activated from GIER via circuits build into BS. Special interface circuitry for each PD connected can be build into BS to suit the special requirements of the various types of PDs. These circuits are described elsewhere.

A register for collecting one whole word is included in this interface circuitry to permit word-by-word transfers where the PD itself is only capable of executing character-by-character transfers.

SECTION 2 - - TERMINOLOGY

The following definitions, terms, and abbreviations are used in this description.

PD	<u>P</u> eripheral <u>D</u> evice
CS	<u>C</u> ore <u>S</u> tore applying to the 1024 word primary core store in the GIER computer
BS	<u>B</u> uffer <u>S</u> ystem
Buffer	applies to the 4096 word core store of the whole Buffer System from which it is to be distinguished
<u>Registers</u> <u>in GIER</u>	R -- F -- '0' H -- r1 -- r2
<u>Registers</u> <u>in BS</u>	BA0 -- BA1 -- BA2 -- BA3 -- BA4 AD -- TR -- BR
F ₀₋₉	is for instance to be interpreted as register F, positions 0 to 9
IGP	<u>I</u> nter <u>G</u> ate <u>P</u> ulse
TR	<u>T</u> ransfer <u>R</u> egister
BR	<u>B</u> uffer <u>R</u> egister
r2	Address Register
LC	Inductor Capacitator
RC	Resistor Capacitator
Set	flip-flop to the 1 position
Reset	flip-flop to the 0 position

SECTION 3 -- CHARACTERISTICS

3.1 Power Supply

BS and associated interface circuitry has a build-in power supply. Input is 3 x 380 V (phase to phase) with common and ground. Maximum load is ca. 1 KW when the interface circuitry for the four PDs is installed.

3.1.1 Input

3 x 380 (± 10 o/o, phase to phase 50 Hz), common and ground

3.1.2 Power Input

1000 W maximum

3.1.2.1 Output

Regulated DC voltages: 5 adjustable: +24V, +8V, -8V, -16V,
-24V (1 o/o)

3 fixed: +1.6V, -1.6V, -3.2V (10-15 o/o)

3.1.2.2 Power Supply Sequence

(See Figure 3-1-2-2 on page 3-2).

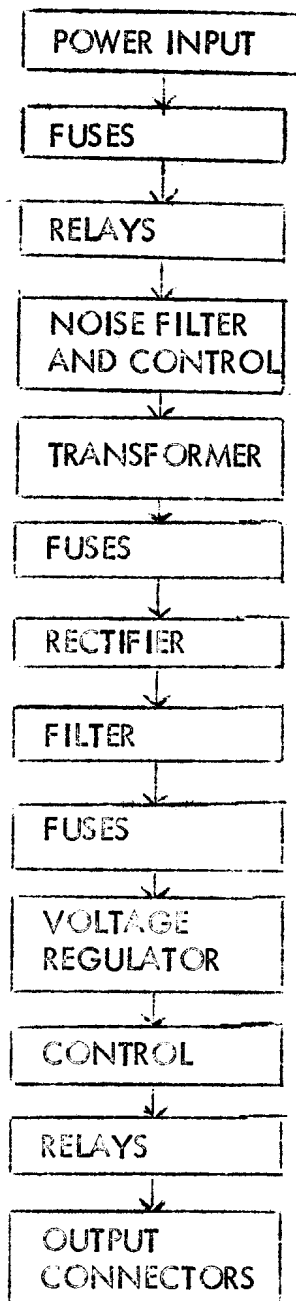


Figure 3-1-2-2. Power Supply Sequence

3-2

3.1.3

Power Input

The symmetry of the three-phase power supply is controlled by a capacitive bridge which simultaneously acts as a noise filter and protects the rectifier diodes against shocks when the mains are disconnected. If there is no symmetry the RA relay switches off the mains relay KA.

3.1.4

Rectifiers

The transformer has five Y-coupled secondary windings which drive five three-phase bridge rectifiers, each of which is protected against overload by three fuses.

3.1.5

Filter

Directly at the output of the rectifier there is one μF capacitor to take out the commutation peaks and hold storage after which a normal LC filter removes the remaining AC component. The LC filter is followed by a fuse.

3.1.6

Voltage Regulators

The adjustable regulators are series regulators with negative feedback and zener diode reference. A bridge circuit checks that all regulated voltages are present and at the same time protects the regulators against overload due to shortcircuiting.

The reference of the -16V regulators is connected to -1.6V . All of the other reference regulated voltages are connected to ground. The fixed voltages are obtained as voltage drop across silicon diodes.

3.1.7

Output Relays

The fixed voltages are always connected to the output connector. The regulated voltages are connected to the output connector via two relays which are controlled from the voltage control circuit.

3.1.8

Voltage Control

-24V, -16V, -8V, +8V, and +24V are controlled by three bridge circuits controlling a flip-flop which in turn controls the output relays via yet another relay. When the power is switched on, the flip-flop is set by an RC circuit, but ten seconds later another, amplified RC circuit reset the flip-flop.

3.1.9

Output Connectors

The load is connected by five 30-poled connectors situated at the top of the power supply unit.

3.1.10

Control Panel

<u>lamps</u>	POWER ON	power on at the mains
	ALARM	voltage control flip-flop set
	LOAD ON	voltages present at output connectors
<u>push-buttons</u>	ON	switch power input on
	OFF	switch power input off
	RESET	reset voltage control flip-flop
<u>toggle switch</u>	LOAD ON	switches voltage at output connectors on/off

3.1.11 Voltmeter

The voltmeter, which is graded in percentages of the nominal voltages, may be switched to measure the voltages on either side of the relays. This makes it possible to check that there is no voltage drop across the output relays.

3.2 Environmental Conditions

3.2.1 Cooling

Cooling is accomplished by the action of built-in fans. A fan is also situated underneath the power supply unit.

3.2.2 Temperature Limits

The temperature inside the cabinet should be maintained at about 20°C ($\pm 3^{\circ}$ during operation), with temperature variations within the cabinet of not more than 3°C .

3.2.3 Air Filters

All the above-mentioned fans are equipped with filters.

3.3 Maintenance

3.1 Inspection

Voltages on both sides of the output relays should be checked daily, and the air filters should be checked according to dust accumulation.

3.2 Cleaning

The airfilters and the relays should be cleaned when necessary.

3.3.3 Adjustments

The adjustable voltages may be regulated by potentiometers on the control panel.

Currents in the Buffer should all be set to 200 mA, but the optimum value is dependent upon temperature.

The constant-current generators are adjustable by means of potentiometers. The inhibit pulse current is set to 200 mA by adjusting -16V so that it is not always possible to maintain this voltage at 100 o/o.

SECTION 4 -- THE IL AND US INSTRUCTIONS

4.1

General

The IL instruction transfers data from a PD to the Buffer or from the Buffer to CS whereas the US instruction transfers data from CS to the Buffer or from the Buffer to a PD.

The three least significant digits of the final address indicate which PD is to be activated. Zero always refers to CS while the other numbers refer to that PD to which the corresponding number has been assigned by means of a unit selection dial. (Dials are situated on each PD). Decoding of these three bits of the final address takes place in BS with reference to the settings of all the unit selection dials to determine the appropriate Transfer Channel to be used. The remaining bits of the final address are transmitted to the interface circuitry of the PD in question. The contents of R prior to execution of an IL/US instruction act as parameters for these instructions and should be set appropriately prior to their execution. F:25 indicates the direction of transfer and is set appropriately during decoding of IL/US.

The PD selected is activated by the BS circuits. When a PD is activated the BS remains passive with respect to the PD until word is transferred from the PD to the interface circuitry, at which time the PD activates the BS circuits.

As long as a PD is active it sends a BUSY signal via BS circuits to GIER.

4.2

The Microprograms for IL and US

Refer to the microprogram table and the block diagrams.

There are special outputs from GIER in the form of emitter follower amplifiers from r2 and '0'.

Special inputs to '0' through gates situated at card 0276 are placed in GIER sections B6-27 to B6-31, and B6-42 to B6-47.

In mode 1 of execution of the microprograms the final address in the instruction is transferred to r2 and F:25 is set according to the operation, viz. 0 for IL and 1 for US.

After this the contents of r2 and F:25 are investigated to determine the type of operation.

If r2:0-9 equals 0, a transfer between CS and the Buffer is to be executed.

If F:25 equals 0 and r2:1 equals 1, a sense-busy instruction (IL 256) is to be executed.

In all other cases a transfer between the Buffer and the other PDs will be executed.

4.2.1

Sense-Busy Instruction (r2:1 = 1 and F:25 = 0)

If r2: 7-9 equals 0 and if either the typewriter, the punch, or the line printer (if connected) are busy, then the instruction(s) in cells up to and including the next RH half-cell will be skipped.

If r2: 7-9 does not equal 0 and if the PD indicated by these positions is busy, then the instruction(s) in cells up to and including the next RH half-cell will be skipped.

4.2.2 Transfer Between CS and the Buffer (r2:0-9 = 0)

4.2.2.1 Transfer of Parameter Information

R:0-9 is transferred to r1:0-9 (indicates start address in CS)
R:10-19 - - F:10-19 (- number of words in transfer)
R:20-39 - - '0':20-39
F:25 - - BA0:00 (- direction of transfer)
'0':28-39 - - BA0:0-11(- start address in Buffer)

4.2.2.2 Transfer from the Buffer to CS (BA0:00 = 0)

A signal, Set CO, is emitted indicating that GIER is ready to receive one word. All positions in '0' (0-41) are set to one. Zero positions are then gated in from the Buffer to GIER via card 0276 by the synchronizing impulse D0.

4.2.2.3 Transfer from CS to the Buffer (BA0:00 = 1)

The contents of R are stored in H.

The contents of L are then transferred via R and '0' to the Buffer. (R is used as an intermediate store to allow drum transfers to take place simultaneously with Buffer transfers).

4.2.3 Transfer Between the Buffer and Other PDs (r2:7-9 ≠ 0)

r2:7-9 is decoded with reference to the settings of the unit selection dial to determine the appropriate BA register and Transfer Channel.

r2:2-6 is fed to the interface circuitry of the PD in question.

'0':8-19 is fed to the interface circuitry of the PD in question.

'0':28-39 is stored in the appropriate BA register (positions 0-11).

F:25 is stored in the appropriate BA register (position 00).

A BUSY signal from the PD in question is gated through to GIER which cycles in the microprogram until the PD no longer is busy. A Set AOK (Address Word Okay) signal is gated through to the PD in question where it is amplified and used for storing addresses, start etc. In BS Set AOK gates the start address into the appropriate BA register. When the PD has received the Set AOK signal it sends the BUSY signal until it has completed the operation.

SECTION 5 -- THE OPERATION OF THE BUFFER SYSTEM

5.1 Transfer of Data

Refer to the microprogram and block diagram.

BS has five 42-bit inputs and one 42-bit output. The power load is distributed by two sets of amplifiers with parallel inputs and two sets of outputs. The one set of amplifiers takes PDs 1-3, the other set PD 4 and GIER. As far as data transfer is concerned GIER may be regarded as another PD.

5.2 AOK Distribution and BUSY Signal Gating

The three bits from r2:7-9 are decoded. The eight outputs are numbered 0-7 and are used for gating the BUSY signal from the PD through to GIER and for gating AOK out to the PD interface. The gated AOKs are fed through two amplifiers: output from the first is fed to the PD interface while the other is used to gate the start address to the appropriate BA register.

5.3 Numbering

The circuits in the Priority System, the address registers, and the Transfer Channels are numbered 0, 1, 2, 3, and 4. Zero always refers to GIER, 1-4 to the PDs. The Priority System gives highest priority to the PDs connected to the Transfer Channel having the highest number.

5.4 The Priority System

All transfers of data are controlled by the Priority System, and from this point of view GIER may also be regarded as a PD with unit number zero. When a PD is activated it assumes control of the data transfer.

When the PD is ready to send or receive a word (information regarding the actual direction of transfer being stored in both the PDs and BS), it gives the C signal to the Priority System. Upon receipt of this the Priority System returns the A signal. If BS is busy nothing happens to the PD. When all activity involving a PD of higher priority has been completed, the following occurs.

If the PD is sending, a word from the PD is ready on the output lines from the moment the A signal is given. The B signal gates this word to the Buffer via TR. If the PD is receiving, on the B signal a word is taken out of the Buffer via TR and BR and transferred to the output lines. When it is available here the D signal is given to the PDs where, after being amplified, it acts as an IGP (input gate pulse).

All incoming C signals wait in the A flip-flop until there is no active B signal with a higher priority number. Only one B signal can be active at a time. The B signal is used to activate the Buffer and is gated with the PD number for selecting and advancing the appropriate address register.

The D signal, \overline{DQ} (\overline{D} zero for transfer from the Buffer to CS), is made in a slightly different manner due to timing restrictions in GIER.

5.5

Address Registers

The Buffer is addressed from AD:0-11. For each Transfer Channel there is a BA register. When an IL or a US instruction is executed, the start address in the Buffer is stored in the appropriate BA register, which is advanced by one every time a word has been transferred. AD:0-11 receives its contents from a BA register immediately before transfer to/from the Buffer takes place.

5.6

Decoding and Current Drivers

The circuits for decoding the address and drive in the Buffer are divided into two identical groups, one for the X wires and one for the Y wires, each group being controlled by six bits in the AD register (originally BA:0-11). The six bits are divided into two groups of three bits each which are decoded, each decoding having eight outputs. These two groups containing eight signals each are connected to two sets of amplifiers, one for reading and one for writing.

Two sets of coordinate decoders, 8 x 8 (one for the read pulse, one for the write pulse) with their outputs coupled in parallel, control the 64 X wires of the Buffer matrix. The Y wires are controlled by the other six bits in the AD register in the same fashion. The currents are kept at a constant value by constant-current generators with high output impedance.

The decoding of the three bits is distributed between two printed circuit cards, the one set of eight outputs being called RA for reading and WA for writing (on card 1002), while the other set of eight is similarly called RB and WB (on card 1003). The latter generates the base current for the driver outputs (on card 1001), while RA and WA inhibit the seven base currents. The current generator is also pulsed. The output transistor during the pulse works in a grounded base circuit.

5.7

The Buffer Matrix Currents

The X and Y currents can be regulated by potentiometers. The inhibit pulse is regulated by adjusting the -16V supply. All currents should be set at 200 mA.

5.8

The Read Amplifier, TR and BR Registers, and Inhibit

The Buffer read amplifiers are coupled to TR through a gate controlled by the strobe pulse. Each flip-flop of TR controls an inhibit pulse amplifier. Data to the Buffer goes directly from GIER and the PDs to five input gates connected to TR. Due to timing restrictions, data from the Buffer goes via BR which has output amplifiers.

To reduce interference from cable capacitors the output amplifiers are doubled, the one connected to Transfer Channels 1-3, the other to GIER and Transfer Channel 4. All these circuits are contained on card 1004.

5.9

Buffer Timing

Bn of the Priority System starts the Buffer timing generator through a short delay element at B22a enabling the address register (AD) to receive a new address before decoding takes place. RT (read time) is set gating the decodings for reading. Next RX (read current X) is set, and short while later RY (read current Y). The duration of these pulses is determined by a delay element at B20a, the trailing edge of which resets RT, RX, RY, and E22a.

RY activates a delay element at B19a, the trailing edge of which triggers B19b, which, dependent on direction of transfer (i.e. the contents of AD:00), generates the strobe pulse or input gate pulse (IGP).

The trailing edge of RX triggers the inhibit pulse. The inhibit generator at B21b controls through amplifiers the inhibit pulse and write time (WT), which gates the decodings for the write currents. The leading edge of inhibit triggers WXY which controls the write currents in the X and Y wires. The duration of WXY is determined by B20b, the trailing edge of which resets the inhibit pulse and WT. To assure that none of the flip-flops in the timing system set for too long a time, there


is an automatic reset which operates if a flip-flop is set for longer than ca. 20 microseconds.

5.10

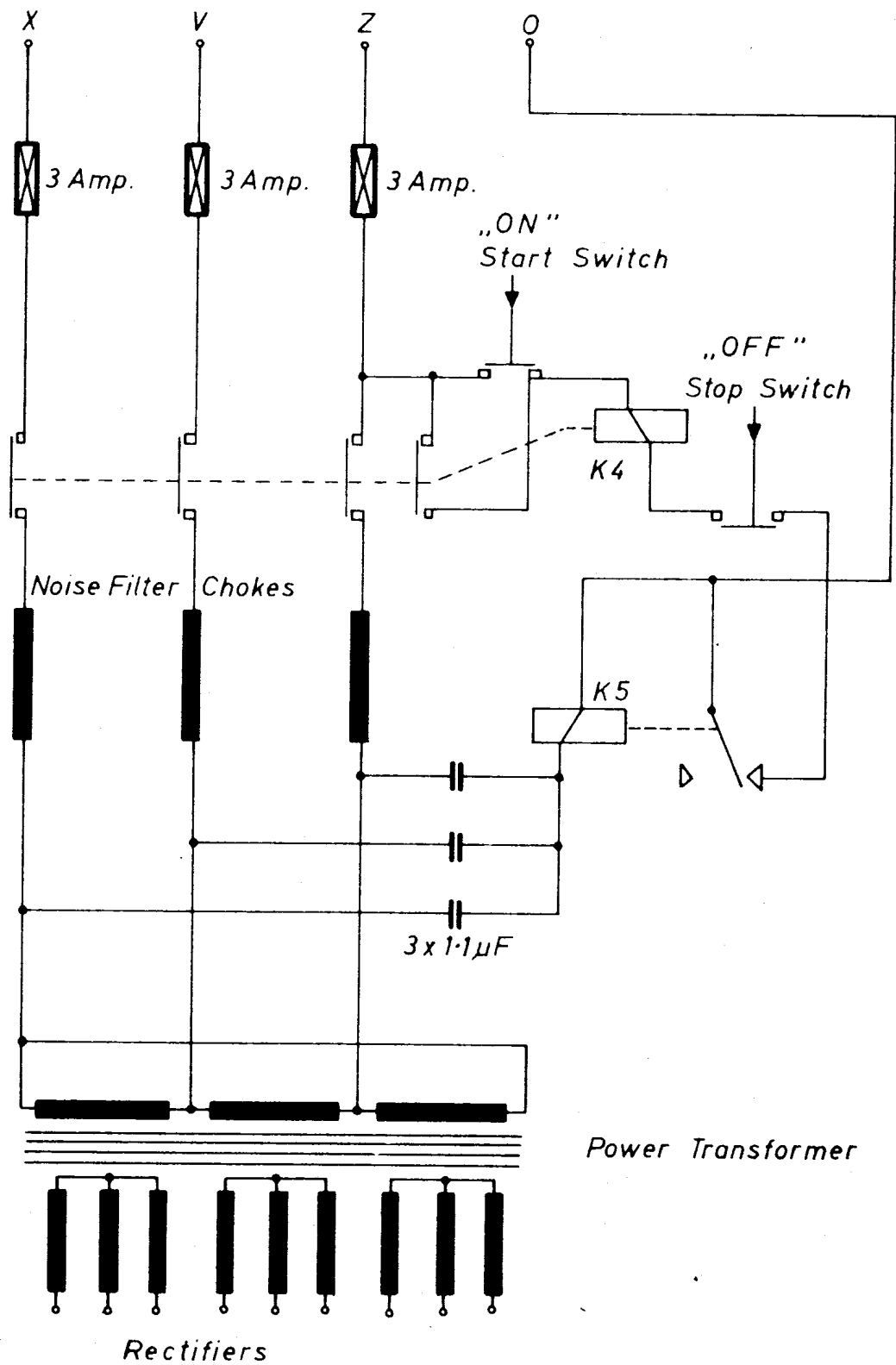
Cable Connections

Ten 60-poled connectors numbered 1-10 connect the Buffer with the PDs and GIER, there being a pair of connectors for each PD (1-2, 3-4, 5-6, 7-8, and 9-10). The even-numbered connectors of each pair contain 42 transfer lines for data transfer from the PDs to the Buffer, plus some lines for control and address signals. The odd-numbered connectors for data transfer from the Buffer to the PDs also contain 42 transfer lines, plus lines for various control and address signals. Connectors 7 and 8 are used for connecting GIER to the Buffer, the others for connecting the PDs to the Buffer. The arrangement of the two groups of 42 data transfer lines is common to all connectors. The arrangement of the remaining 18 lines depends upon the type of PD connected, and therefore only the wiring schedules for connectors 7 and 8 are included in the manual. The wiring schedules for other PDs will be included in the description of the interface circuitry for the PD in question.

PS	1	Power Input
PS	2	Principle of Rectifier With Regulator
PS	3	List of Component Values
PS	4	Diode Voltage dividers
PS	5	Control of Output Connector Relays
PS	6	Voltmeter Switches
PS	7	+24V Regulator
PS	8	-24V — " —
PS	9	-16V — " —
PS	10	-8V — " —
PS	11	+8V — " —
PS	12	Voltage Control
PS	13	Placing of Components
PS	14	Out Connectors

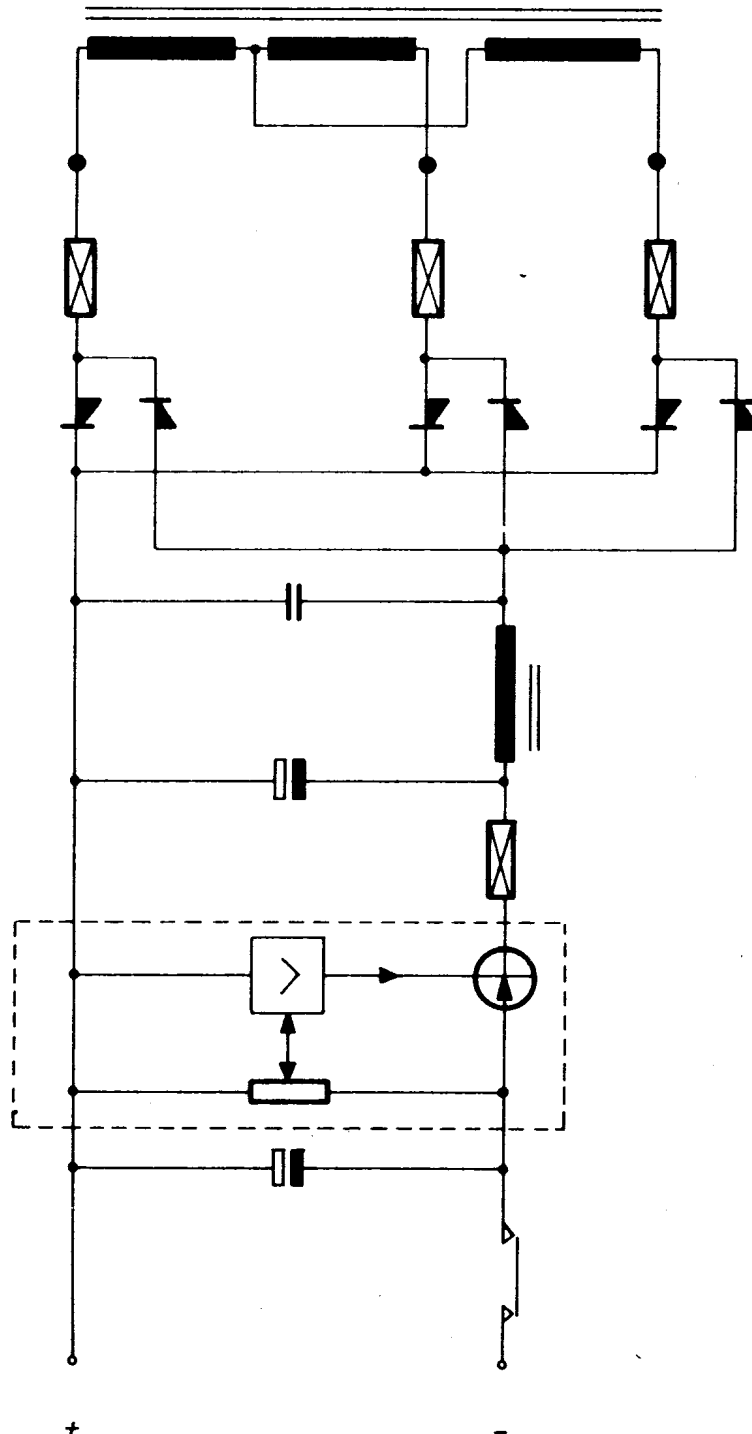
Unit: Buffer Store 	Designed K. H. A.	Power Supply	Drawing No	
	Approved		Drawn by G. T. 7.2.66.	
	Checked 1.2.63.		Checked F. E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			PS 0	

3x 380V
(phase to phase)



Unit: Buffer Store REGNE CENTRALEN	Designed K.H.A.	Power Input	Drawing No	
	Approved		Drawn by G.T. 20.1.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			PS 1	

3 Phase Transformer



Fuses F10-24

Rectifiers

1μF

Choke L

Capacitor C9-C14

Fuses F25-29


Regulator

Capacitor C15-C22


Relay

Unit: Buffer Store	Designed K.H.A.	Principle of Rectifier With Regulator	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.T. 21.1.66	
	Checked 1.2.63		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			PS 2	

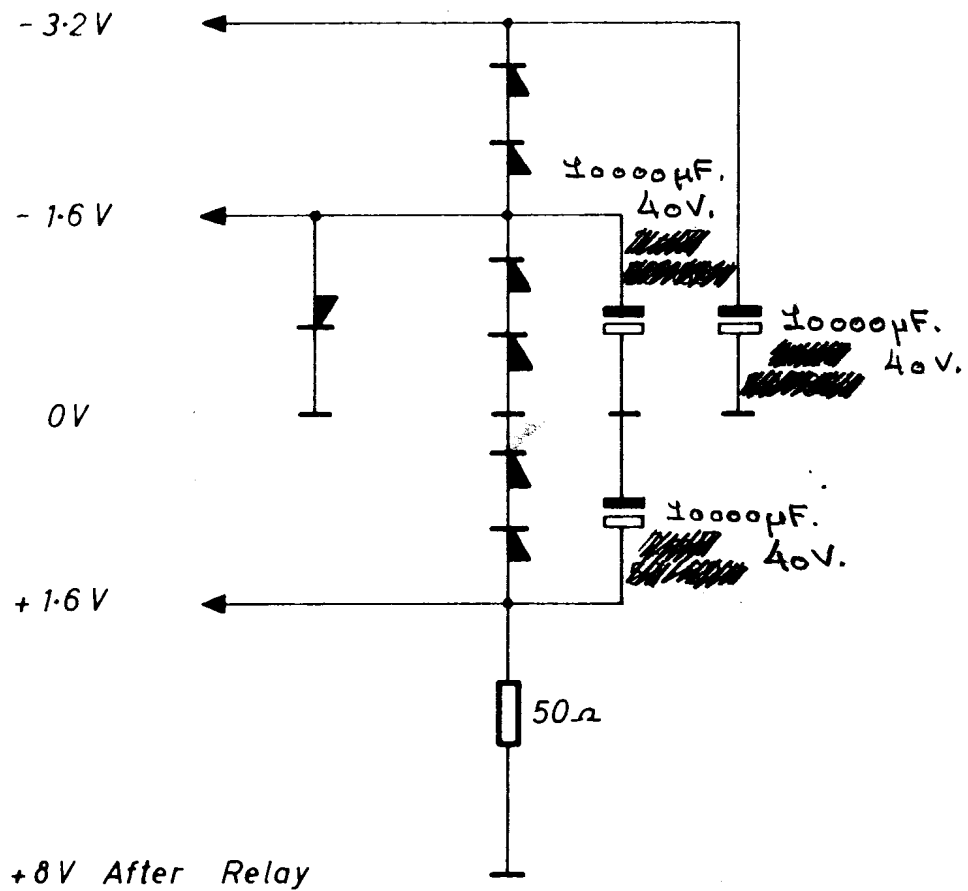
																	18	19	20	21	22	23	24	25
																		1232 -1		1232 -1				
																		Read-Write Current		Read-Write Current				
																	0200 -43	1007 -46	1007 -2	1004 A-1	1008 A-1	1008 A-1	1000 A-1	
																		IGP-TR Stroke	Stroke	Generator Rt Wt	Rt Wt	Rt Wt	Ampl.	Clock Reset
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	1001	1001	1001	1001	1001	1001	1001	1001
Driver Y	Driver Y	Driver Y	Driver Y	Driver Y	Driver Y	Driver Y	Driver Y	Driver Y	Driver X	Driver X	Driver X	Driver X	Driver X	Driver X	Driver X	Driver X	1003 -2	1003 -2	1003 -2	1003 -2	1002 -2	1002 -2	1002 -2	1002 -2
Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding Y	Decoding X	Decoding X	Decoding X	Decoding X	Decoding X	Decoding X	Decoding X	Decoding X	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5
TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23
1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1004 -5	1007 -1	1008			
TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	TR	IGP-TR-DR DO-10er	Ampl.			
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39		40	41	42					
1005	1005	1008	1008	1008	1008	1008	1008	1008	1008		1004	1004	1004	1004	1004		1004	1004	1004	1004	1004	1004	1004	1004
-1	A-1	A-1	A-1	A-1	A-1	A-1	A-1	A-1			-4	-4	-4	-4	-4		-4	-4	-4	-4	-4	-4	-4	-4
Gates	Gates	Bn Bn	A4 B4	A3 B3	A2 B2	A1 B1	A0 B0	Ampl.	Ampl.		AD 00	AD 0 Y	AD 1 Y	AD 2 Y	AD 3 X		AD 4 X	AD 5 X	AD 6 X	AD 7 Y	AD 8 Y	AD 9 X	AD 10 X	AD 11 X
0309 -10	1008	1008		1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017
Inverter Ampl.	Priority Ampl.	Ampl. Bn-Bn		BA2 00	BA2 0	BA2 2	BA2 4	BA2 6	BA2 8	BA2 10	BA1 00	BA1 0	BA1 2	BA1 4	BA1 6	BA1 8	BA1 10	BA0 00	BA0 0	BA0 2	BA0 4	BA0 6	BA0 8	BA0 10
0203 -7	1008	0309 -9	1008	0200 -38	1008	0251 -14	0251 -14				1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017	1017
Decoding PD No.	BUSY Gates	AWR Gates	Ampl. AWR	Ampl. AWR	AD7,8,9	+	+				BA4 00	BA4 0	BA4 2	BA4 4	BA4 6	BA4 8	BA4 10	BA3 00	BA3 0	BA3 2	BA3 4	BA3 6	BA3 8	BA3 10
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

Unit Buffer/DFA200		Designed V.!!.	Drawing No	
		Approved	Drawn by M. L. 48.5.6	
		Checked 6.3.68	Checked I.R. 5.4.1968	
		Last Revision	1 Sheets Sheet 1	
Survey of Printed Cards - A,B,C,D,E,F, G,H			BTZ	

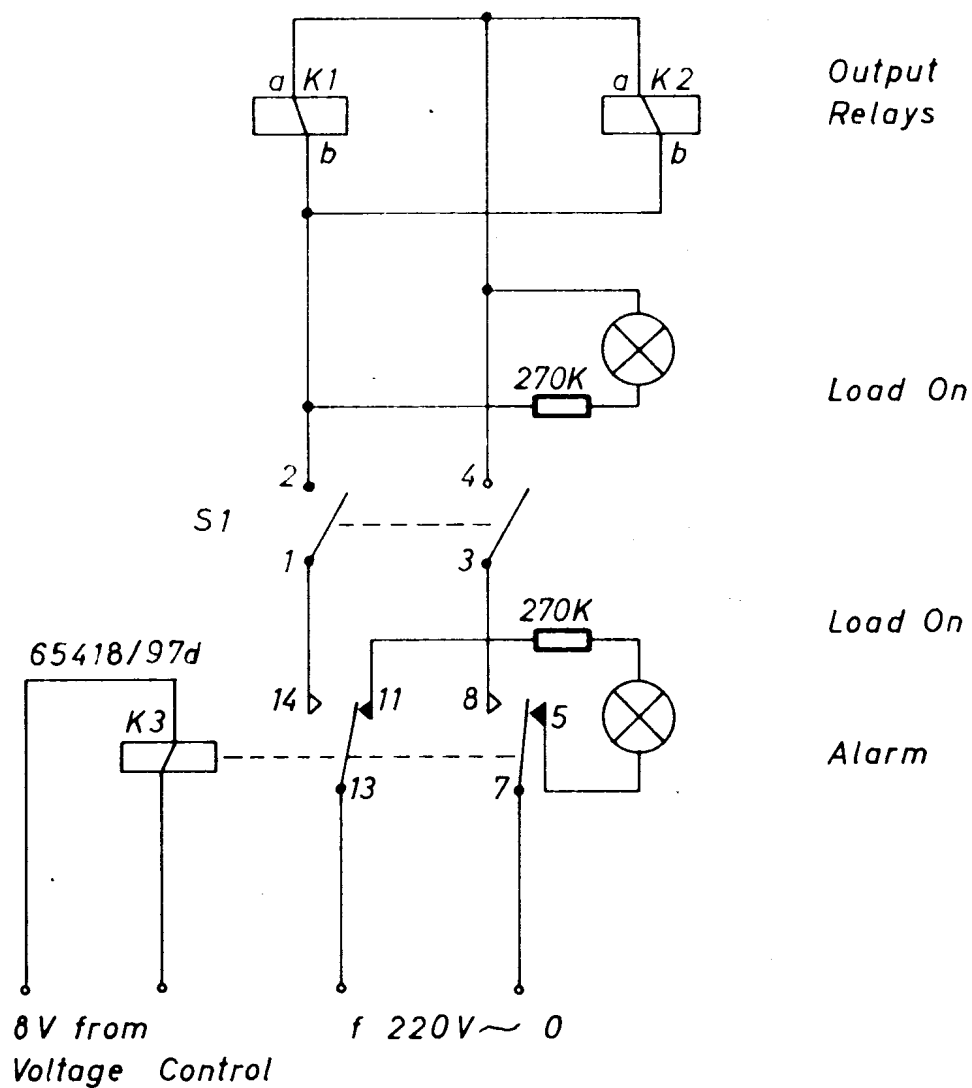
Output Voltage	-24V	-16V	-8V	-3.2V	-1.6V	+16V	+8V	+24V
Rectifier Out Voltage	32V	21V	13V				13V	32V
Max. Out Current	15A	4A	12A	-1A	-1A	0.5A	5A	2A
Fuse In AC Circuit	10A	5A	10A				5A	3A
Filter Choke	10mH	5mH	1.5mH				5mH	10mH
First Filter Capacitor	2x8mF	25mF	25mF				25mF	8mF
Fuse In DC Circuit	10A	5A	10A				5A	2A
Second Filter Capacitor	33000µF	10000µF	33000µF	10000µF	10000µF	10000µF	10000µF	10000µF
Power Transistors	11+1	2	5+1				2	2
Regulator Diodes				2	2	2		
Power Resistors	1x50Ω	4x4Ω	1x50Ω			1x50Ω	4x2Ω	4x6Ω
Power Resistors	20x4Ω		10x2Ω					

Unit: Buffer Store 	Designed K.H.A.	List of Component Values	Drawing No	
	Approved		Drawn by G.Y. T.2.64.	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			PS 3	

All Diodes: 1N 1200



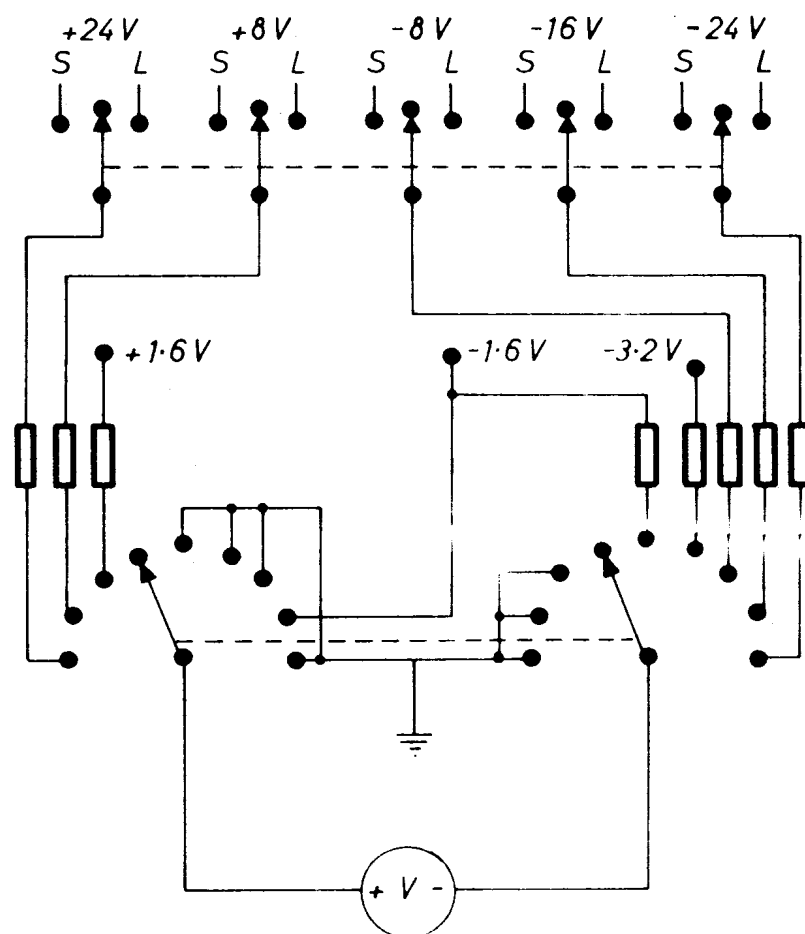
Unit: Buffer store	Designed K.H.A.	Diodes Voltage Dividers	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.I. 26.1.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			PS 4	



Unit: Buffer Store	Designed K.H.A.	Control of Output Relays		Drawing No
	Approved			Drawn by G.T. 26.1.66.
	Checked 1.2.63.			Checked F.S. 19.10.67
	Last Revision			1 Sheets Sheet 1
				P5 5

S: Supply


L: Load

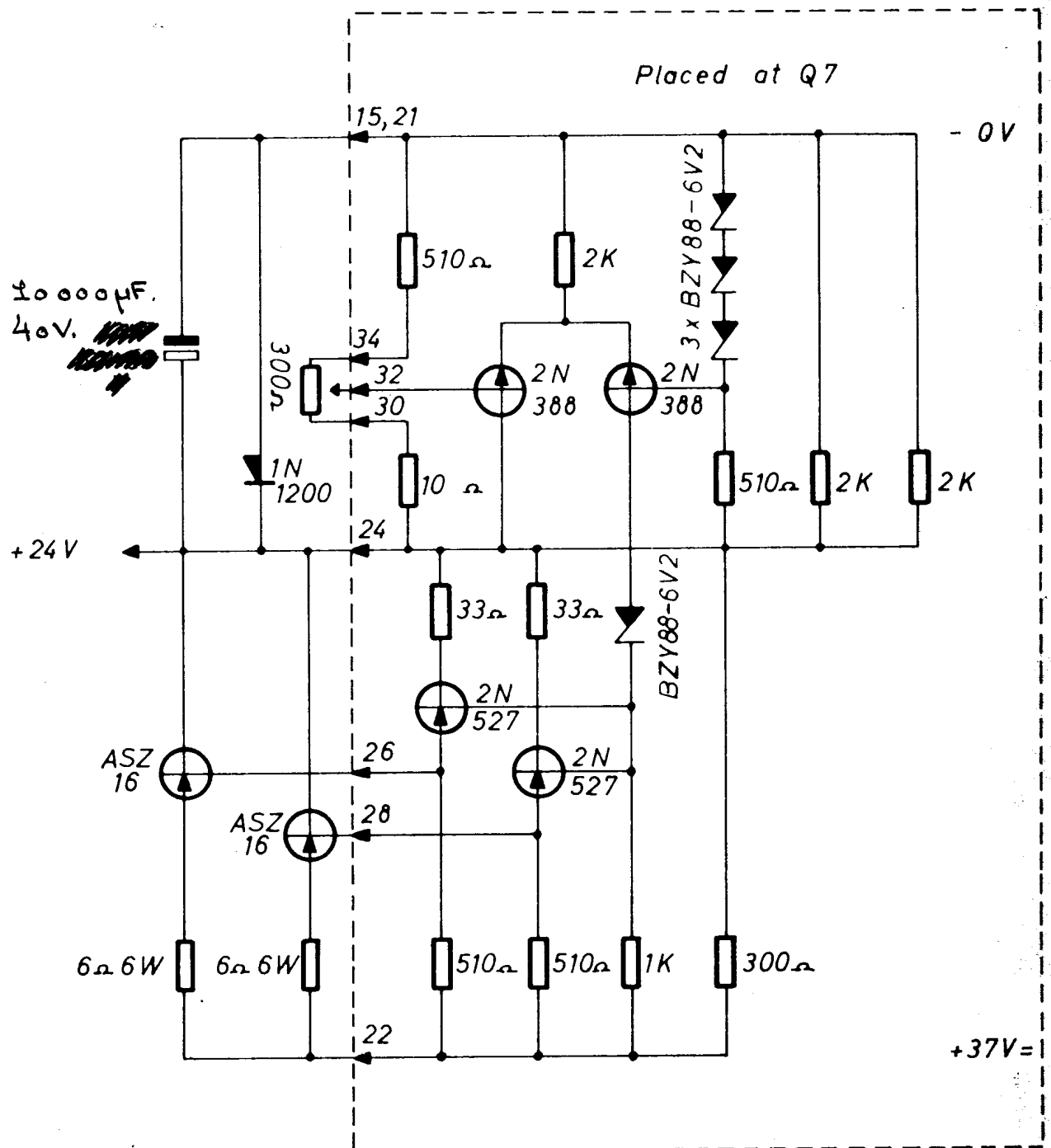


Load On

Range
Selector

Both Switches Shown in Neutral Position

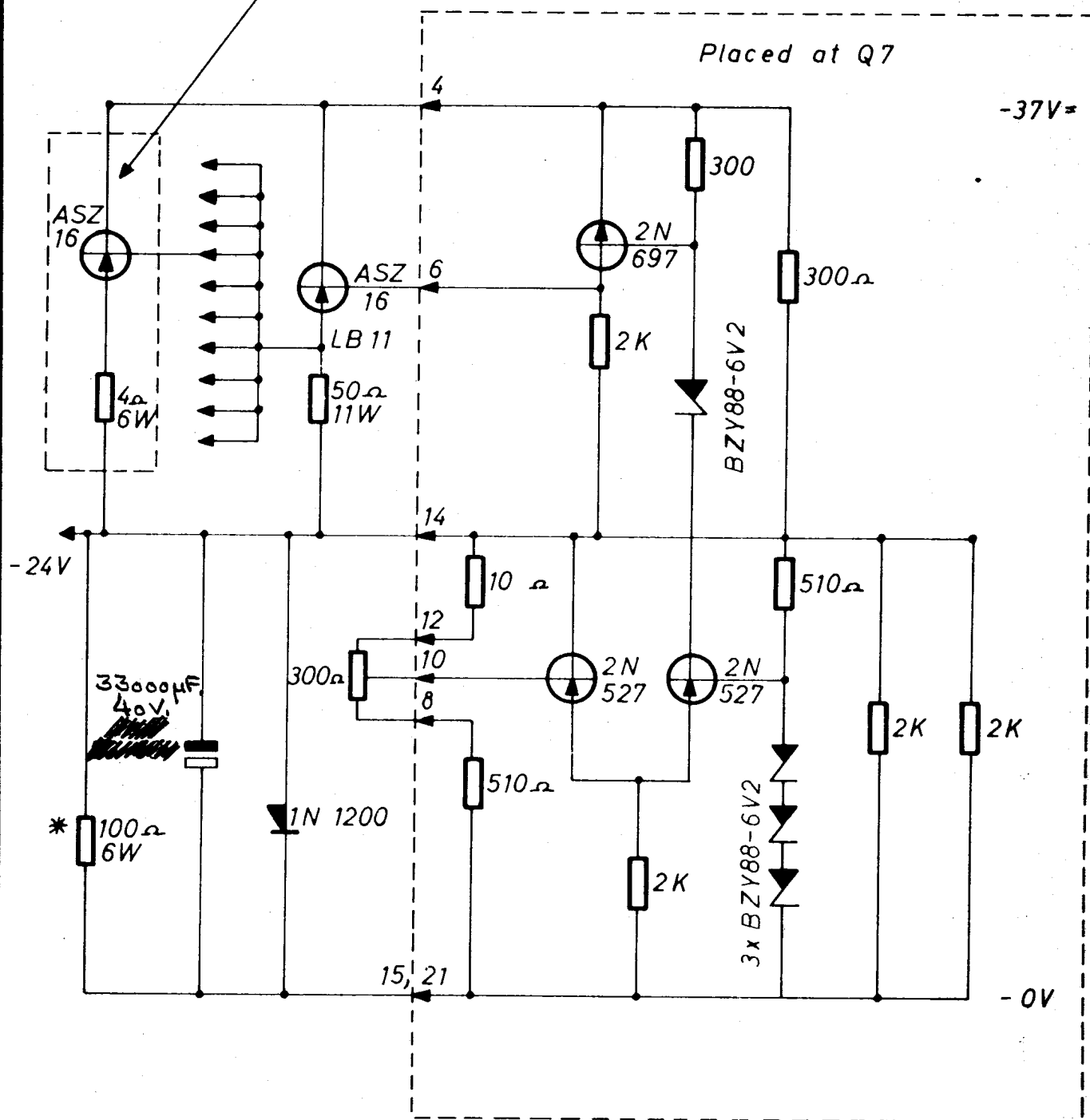
Unit: Buffer Store	Designed K.M.A.	voltmeter Switches	Drawing No.
	Approved		Drawn by J. J. J. J. J.
	Checked 1.2.63.		Checked J. J. J. J. J.
	Last Revision		Screen Free
			FE



Unmarked Resistors: 1/2W

Unit: Buffer Store	Designed K.H.A.	Power Supply +24V Regulator	Drawing No	
I REGNE CENTRALEN	Approved		Drawn by	G.I. 24.1.66
	Checked 1.2.63.		Checked	F.E. 19.10.67
	Last Revision 12.9.67 LL		2 Sheets	Sheet 1
		Q 7	1223-1	PS 7

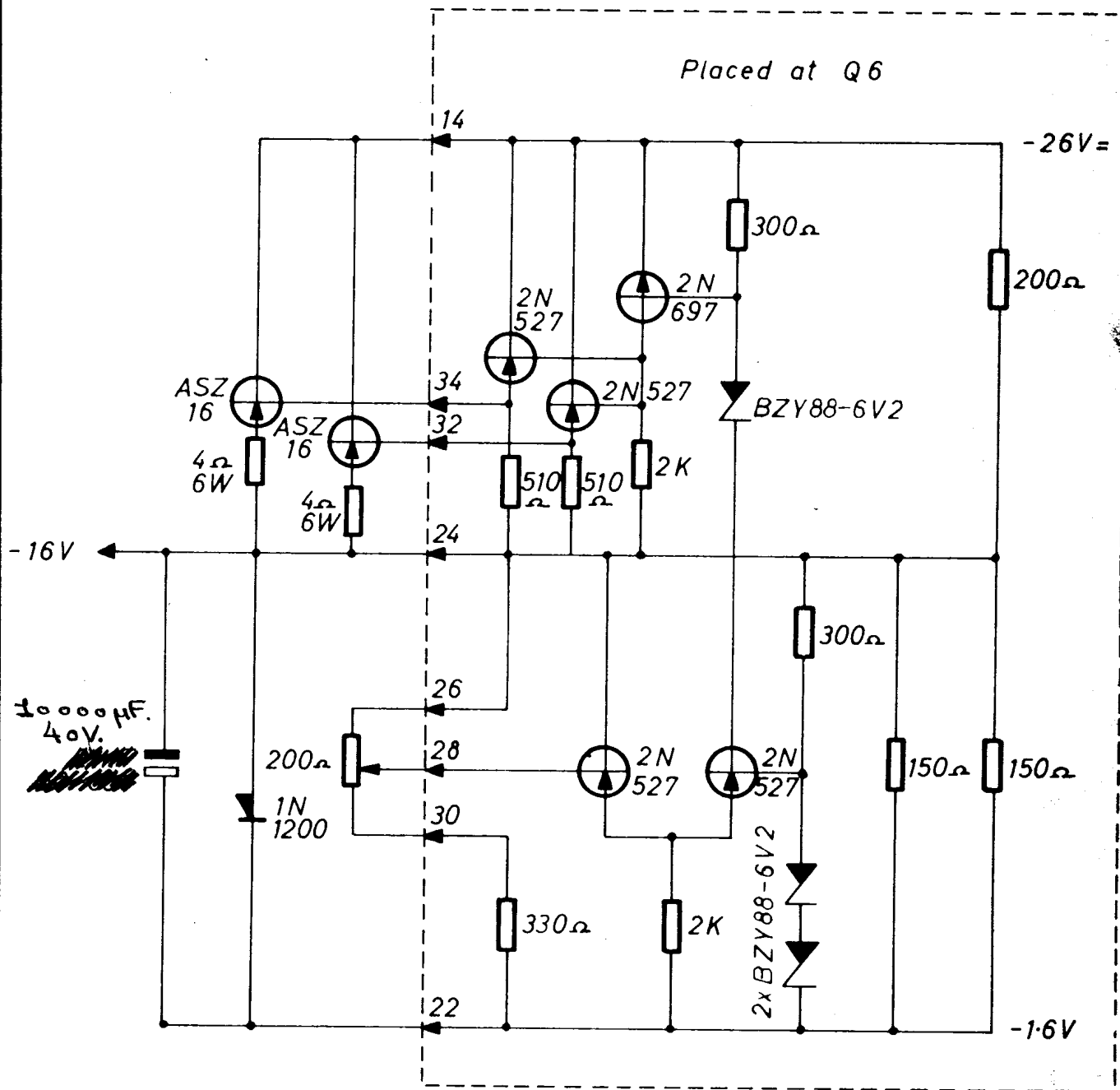
This Circuit Doubled 10 Times



Unmarked Resistors: 1/2W

* Dummy Load under Testing Procedure.

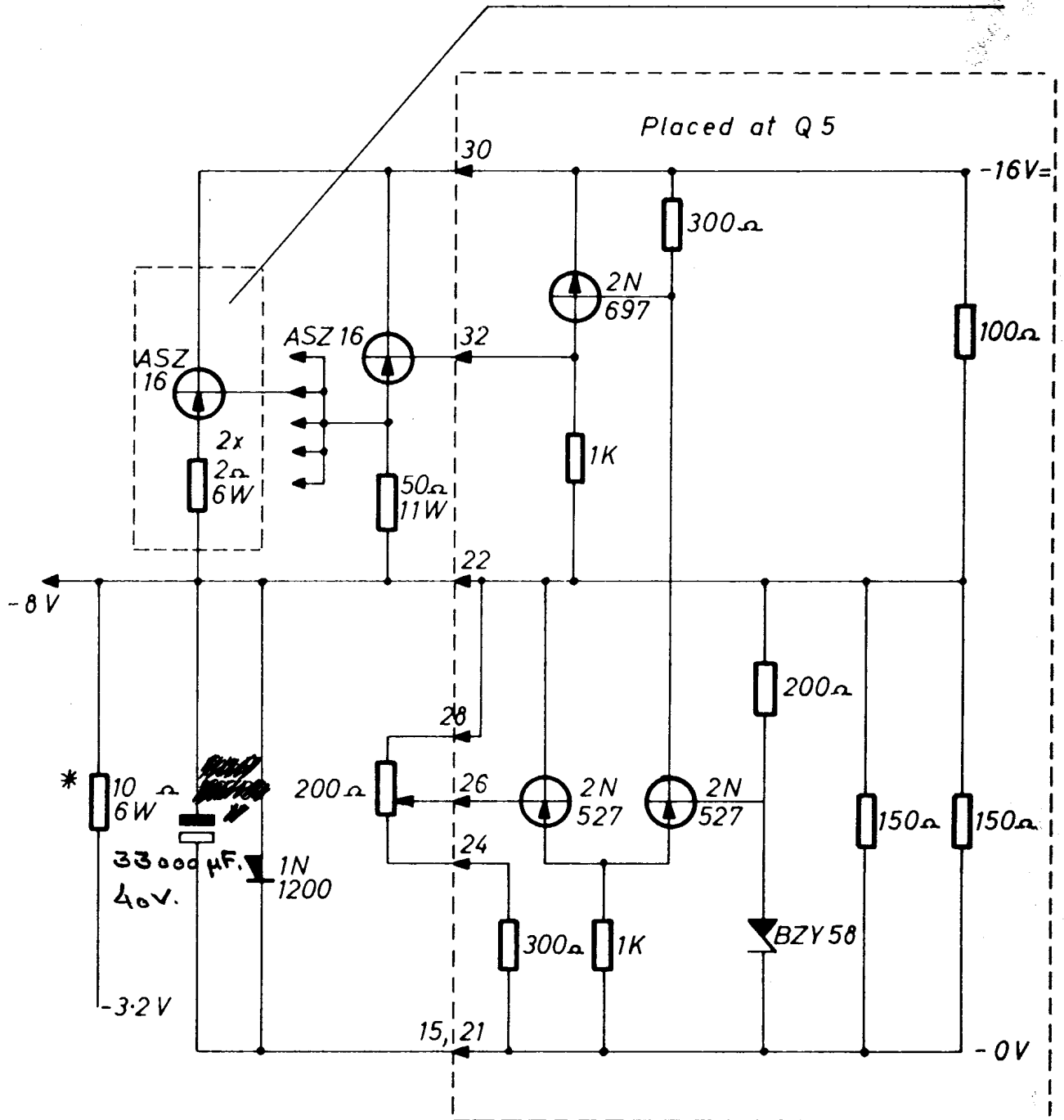
Unit: Buffer Store	Designed K.H.A.	Power Supply	Drawing No
REGNE CENTRALEN	Approved	-24V Regulator	Drawn by G.T. 25.1.66
	Checked 1.2.63.		Checked F.E. 19.10.67
	Last Revision 18.9.67 L.L.		2 Sheets
			Sheet 2
			Q 7
			1223-1
			PS 8



Unmarked Resistors: 1/2 W

Unit: Buffer Store	Designed: K.H.A.	Power Supply -16V Regulator	Drawing No	
! REGNE CENTRALEN	Approved		Drawn by G.T. 25.1.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision 12.9.67 L.L.		1 Sheets	Sheet 1
			Q 6	1221-1
PS 9				

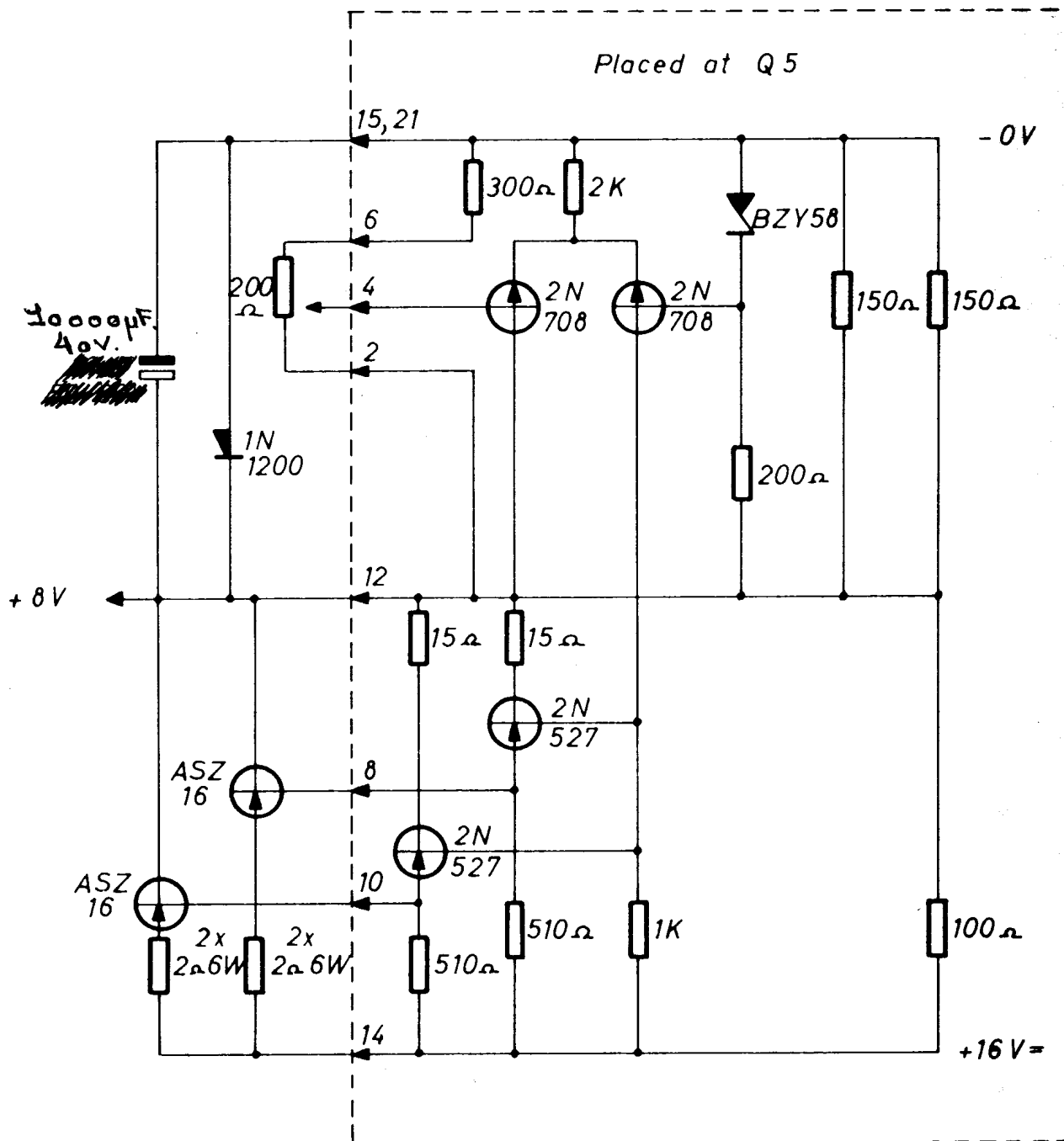
This Circuit Doubled 5 Times



Unmarked Resistors: 1/2W

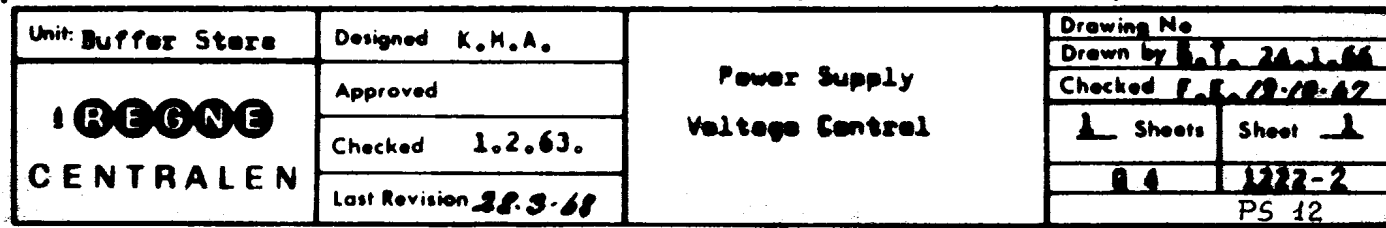
* Dummy Load under Testing Procedure

Unit: Buffer Store	Designed K.H.A.	Power Supply -8V Regulator	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.Y. 25.1.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		2 Sheets	Sheet 1
			Q 8	1220
			PS 10	



Unmarked Resistors: 1/2 W

Unit: Buffer Store	Designed K. H. A.	Power Supply +8V Regulator	Drawing No	
	Approved		Drawn by G. T. 24.1.66	
	Checked 1.2.63.		Checked F. E. 19.10.67	
	Last Revision		2 Sheets	Sheet 2
			Q 5	1220
			PS 11	



C19 - C22 Capacitors

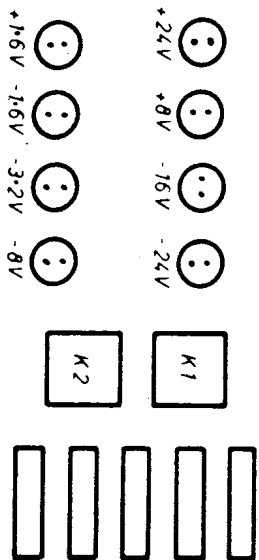
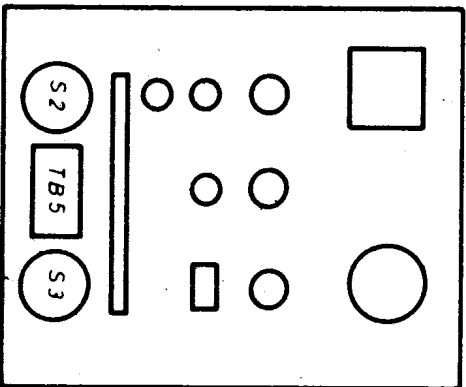
Connector

C15 - C18 Capacitors

Time Counter Voltmeter

Control Panel

Terminal Board
TB 4



Relays K1, K2
Plugs Output

Resistors

Power Transistors
Terminal Board TB1

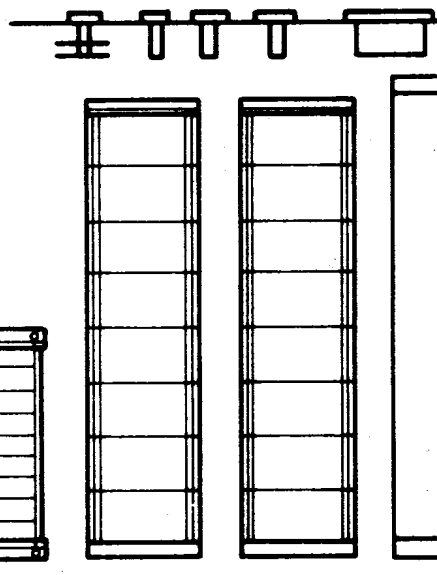
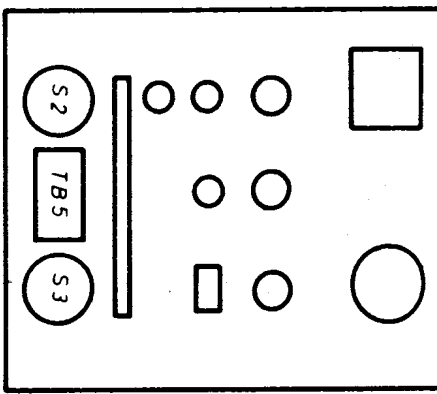
Power Transistors
Terminal Boards TB2, TB3

Diodes TB6

Relay K3

Printed Circuit Board

Control Panel
Terminal Board
TB 4



Power Transistors
Terminal Board TB 1
Power Transistors
Terminal Boards TB 2, TB 3

Diodes TB 6

Relay K 3

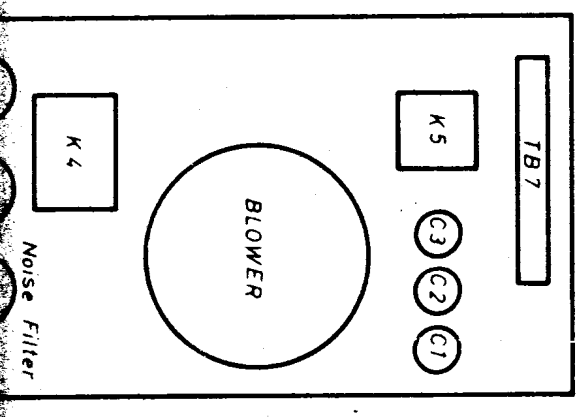
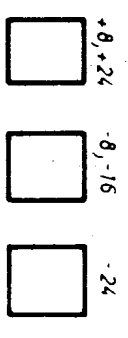
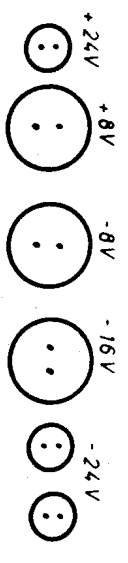
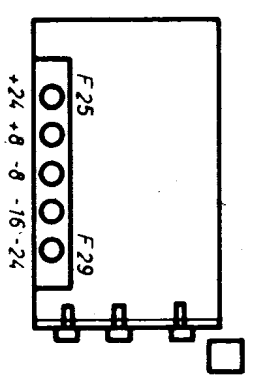
Printed Circuit Cards E
Potentiometers for Vol-
tage Regulation

Fuse F 25 - 29

Electrolytic Capacitors
C 9 - 14

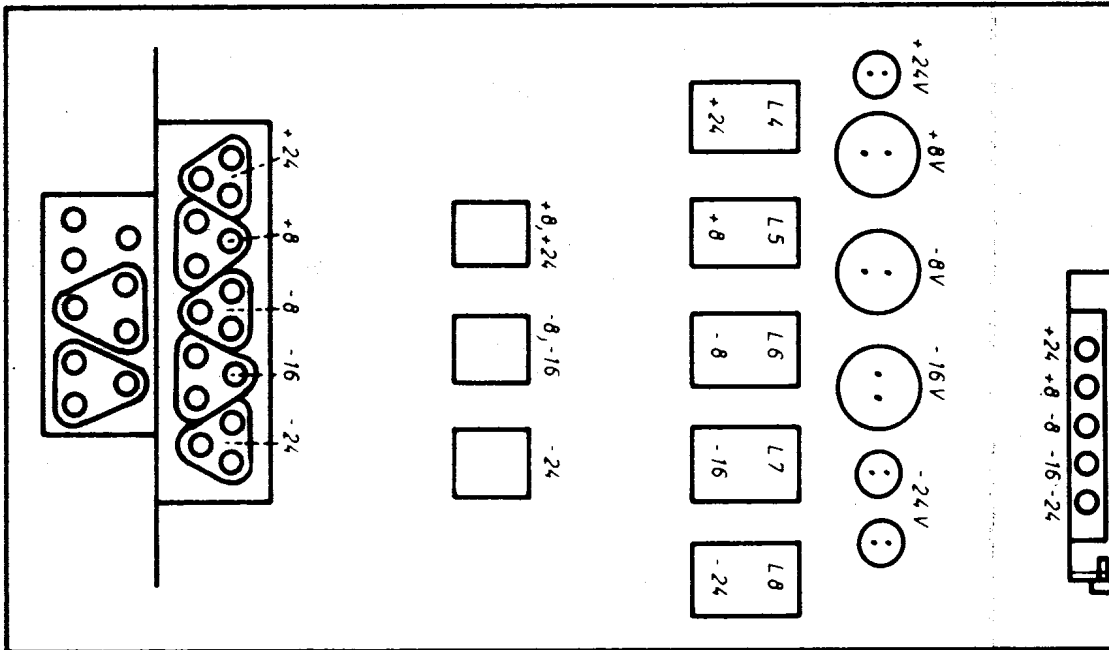
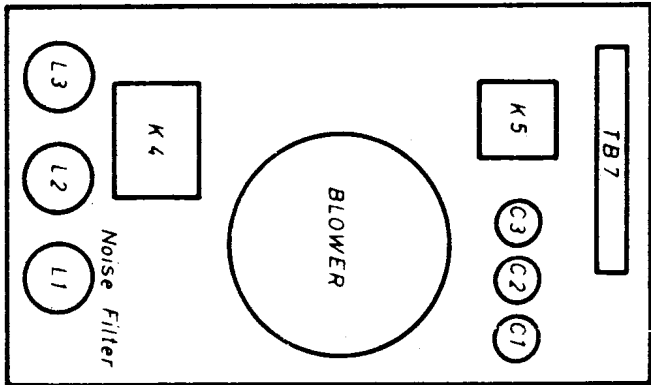
Inductors

Rectifiers CR 1 - 6



Unit: BUFFER STORE	Designed K. H. A.	Approved	Checked 1. 2. 63	Last Revision
CENTRALEN				
REGENE				
PLACING COMP				

PLACING OF COMPONENTS



Fuse F 25 - 29

Electrolytic Capacitors
C 9 - 14


Inductors

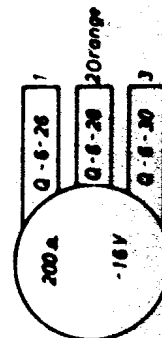
Rectifiers CR 1 - 6

Fuses F 10 - 24

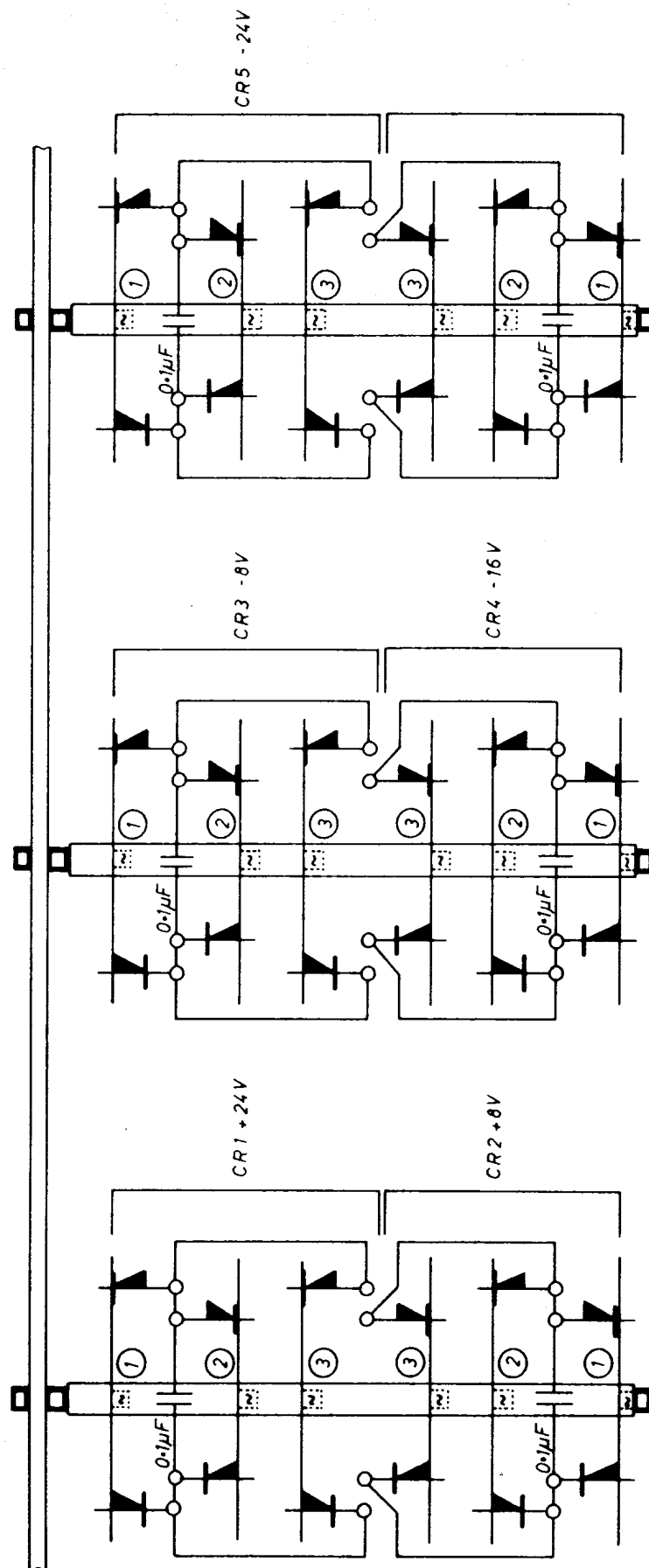
Fuses F 1 - 9

a	b	c	
+24V ●	+24V ●	+24V ●	1
+8V ●	+8V ●	+8V ●	2
+1.6V ●	+1.6V ●	+1.6V ●	3
0V ●	0V ●	0V ●	4
-1.6V ●	-1.6V ●	-1.6V ●	5
-3.2V ●	-1.6V ●	-3.2V ●	6
-8V ●	-3.2V ●	-8V ●	7
-16V ●	-8V ●	-16V ●	8
-24V ●	-16V ●	-24V ●	9
-24V ●	-24V ●	-24V ●	0

Unit: Buffer Store  CENTRALEN	Designed K.H.A.	Out Connectors	Drawing No	
	Approved		Drawn by G.T. 4.2.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			P5 14	



POWER DIODES.



Unit: **BUFFER STORE**

Designed **K. H. A.**

REGNE
CENTRALEN

Approved

Checked **1. 2. 63.**

Last Revision

RECTIFIER STACK.

Drawing No

Drawn by **G. T. 11. 7. 67.**

Checked **F. E. 19. 10. 67**

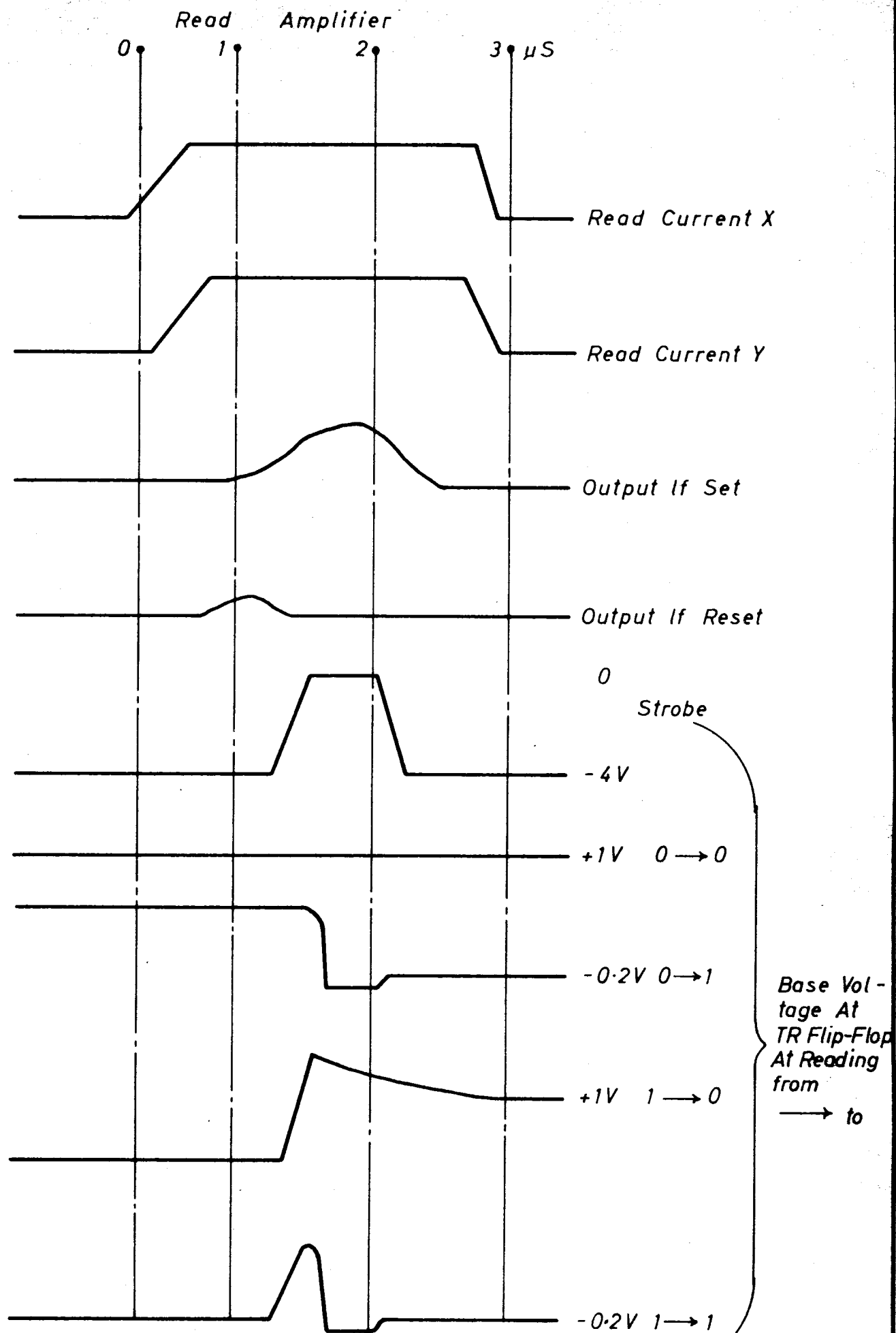
1 Sheets


Sheet 1

1	Q 4-4
2	
3	
4	Q 4-2


¹¹ TB4-6	¹³ TB7-3	¹⁴ TB4-11	¹⁶
¹⁷	⁶	¹⁵	⁹
⁵ TB4-4	⁷ TB7-12	⁸ TB4-12	¹⁰

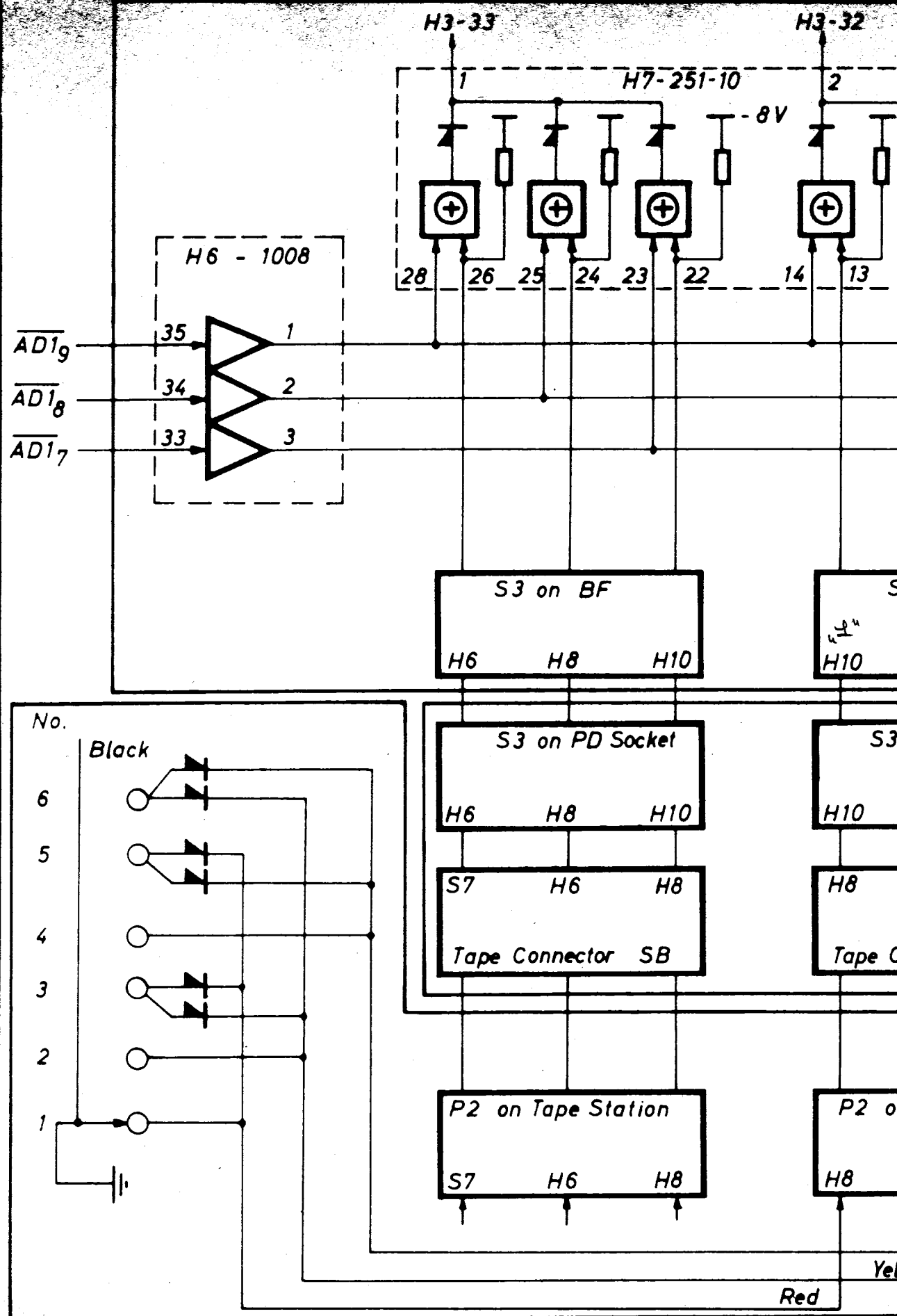
Unit: BUFFER STORE REGNE CENTRALEN	Designed K. H. A.	POWER SUPPLY K 3	Drawing No	
	Approved		Drawn by I. K. 10.7.1967	
	Checked 1.2.63		Checked F.E.	
	Lost Revision		<u>1</u> Sheets	Sheet <u>1</u>

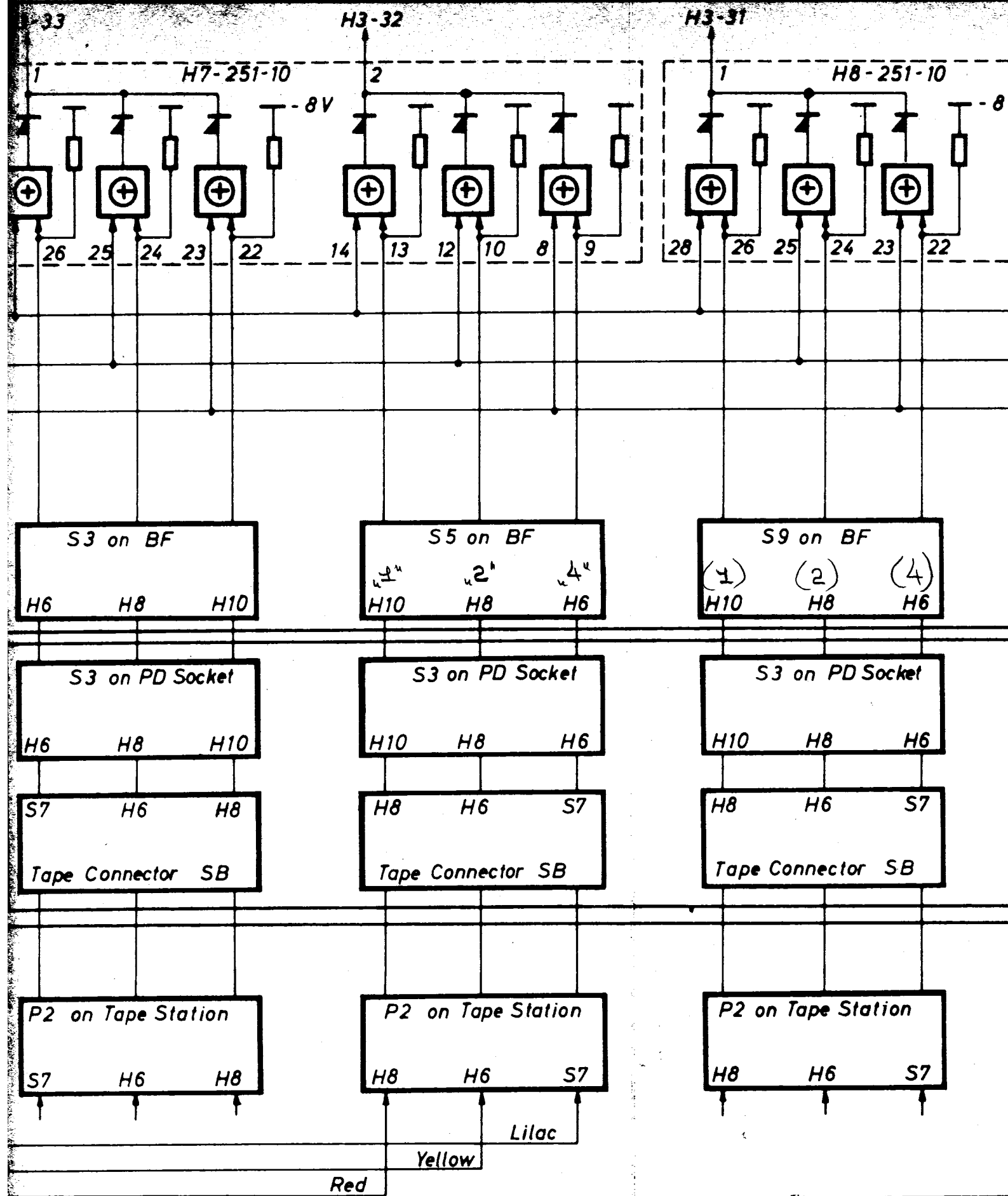


Unit: Buffer Store	Designed K. H. A.	Buffer	Drawing No
 CENTRALEN	Approved		Drawn by G. T. B. 2.66.
	Checked 1.2.63.		Checked F. E. 19.10.69
	Last Revision		<div style="display: flex; justify-content: space-between;"> <u>1</u> Sheets Sheet <u>1</u> </div>

B	1	Data Transfor
B	2	Addres Transfor
B	3	AWR and Busy Distribution
B	4	Prority System
B	5	Synchronizing System GIER-BS
B	6	Address Register
B	7	Address Decoding and Ferrite Drivers
B	8	FL Timing System
B	9	IGP→TR→BR and D0
B	10	Complete System Block Diagram
B	11	Amplifiers for Priority System
B	12	Placing of Printed Circuit Cards

Unit: Buffer Store	Designed K.H.A.	Block Diagrams	Drawing No	
 REGNE CENTRALEN	Approved		Drawn by G.T. 8.2.66.	
	Checked 1.2.63		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			B.D.	





Unit: **Buffer Store**

Designed V.H.

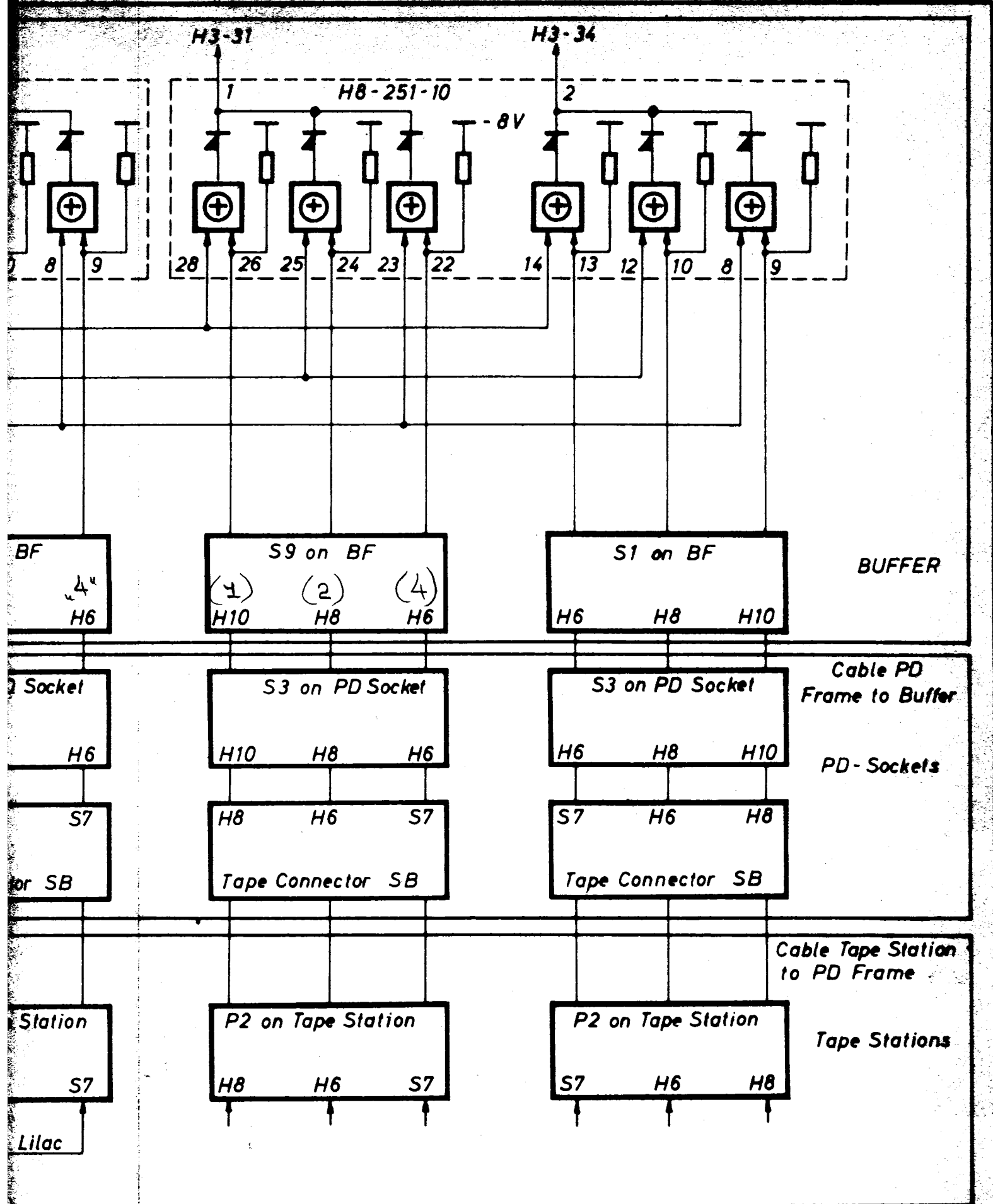
IRGNE

Approved

CENTRALEN

Checked 1.2.1964.

Last Revision



Unit: **Buffer Store**

Designed V.H.

REGNE
CENTRALEN

Approved

Checked 1.2.1964.

Last Revision

Arrangement of PD Selection.

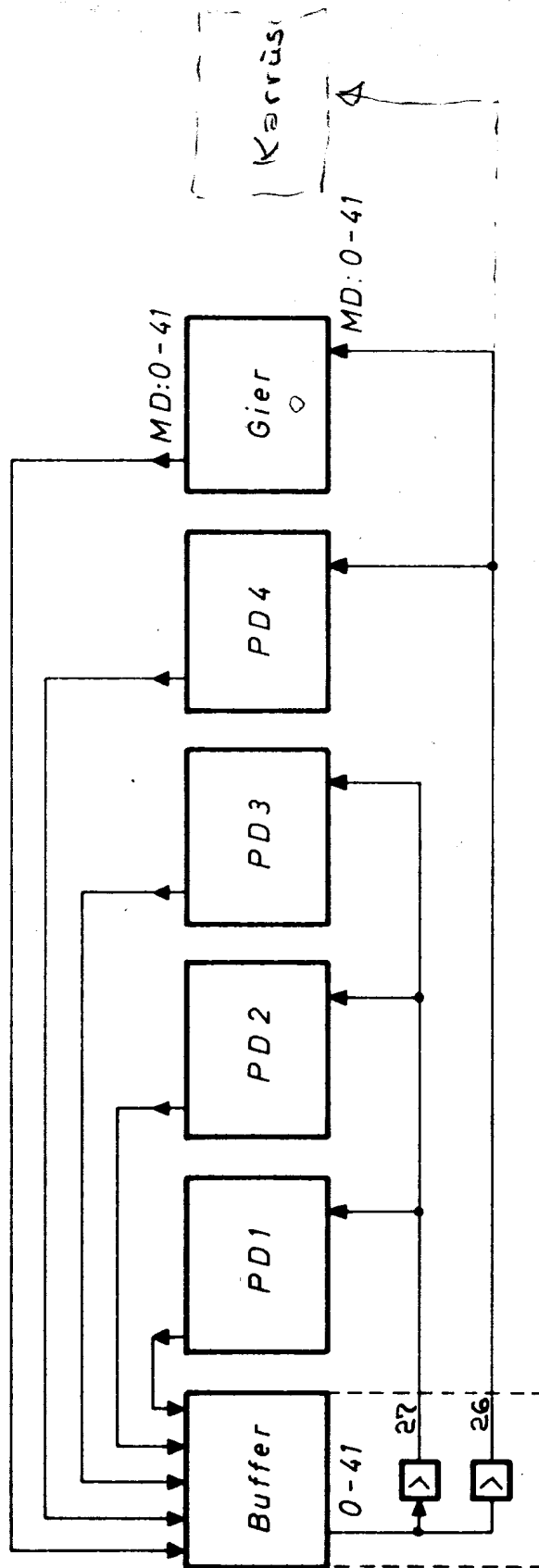
Drawing No


Drawn by I.K. 3.11.1962.

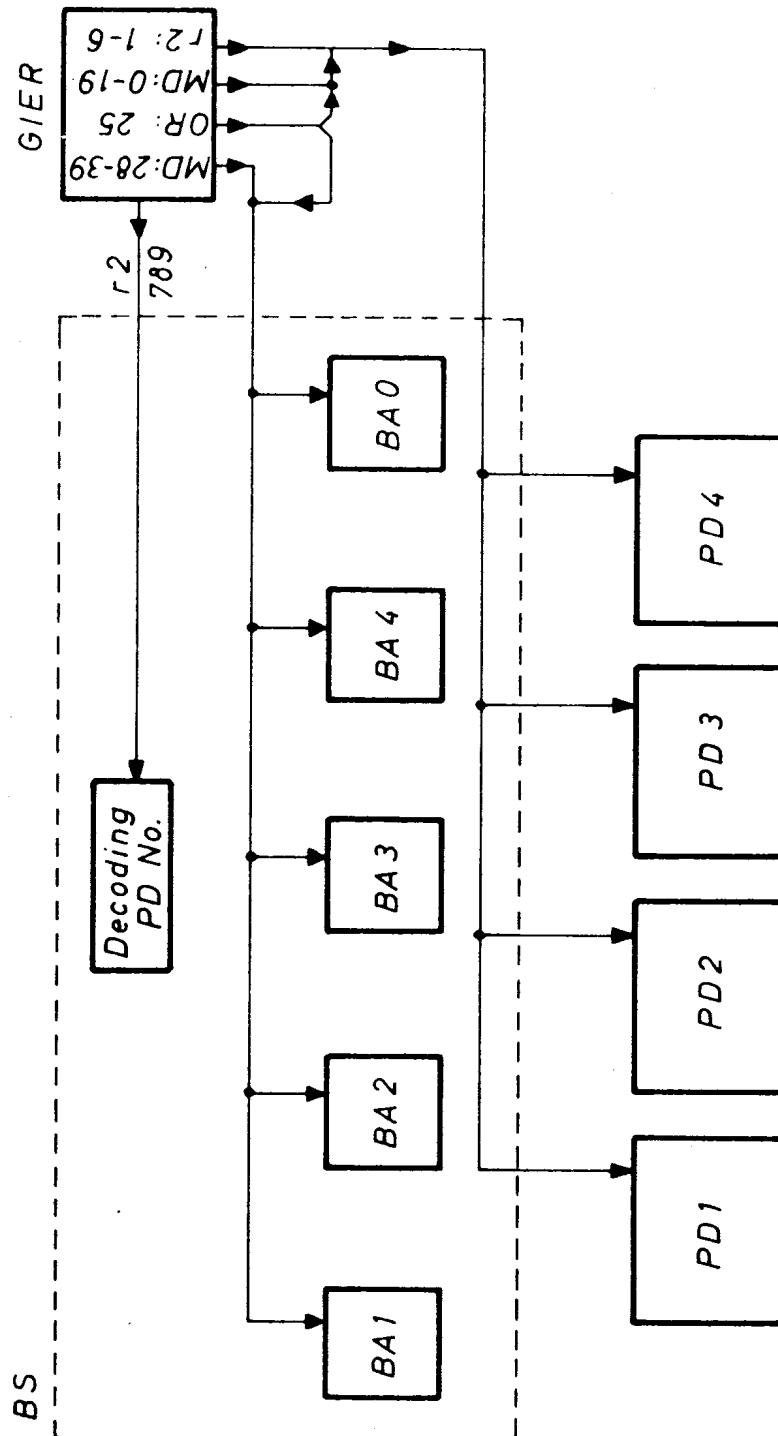
Checked F.E. 6.11.1962

1 Sheets

Sheet 1

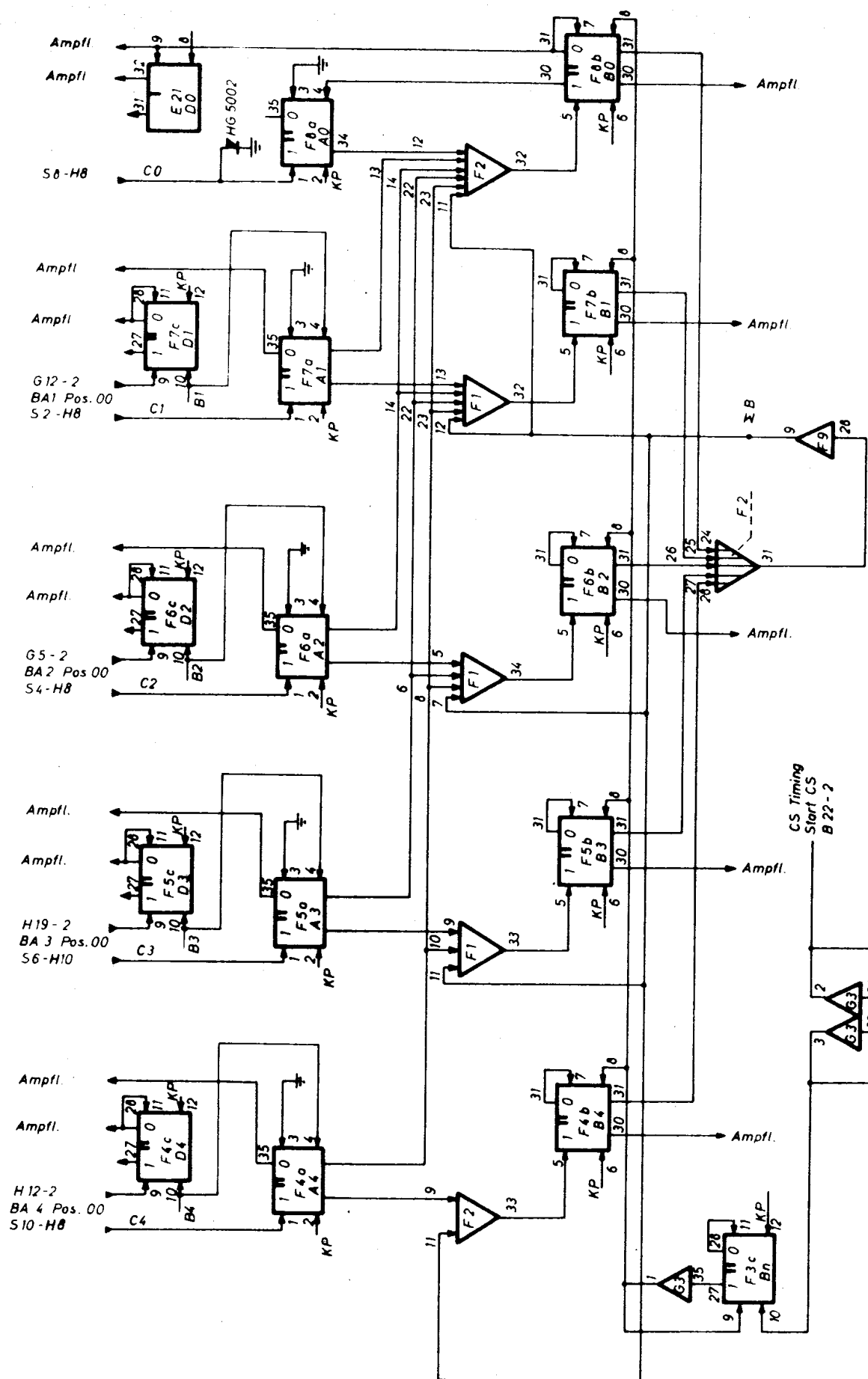



Unit: Buffer Store	Designed K.H.A.	Data Transfer.	Drawing No	
	Approved		Drawn by G.Y. 20.1.66	
	Checked 1.2.63		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
CENTRALEN			B 1	



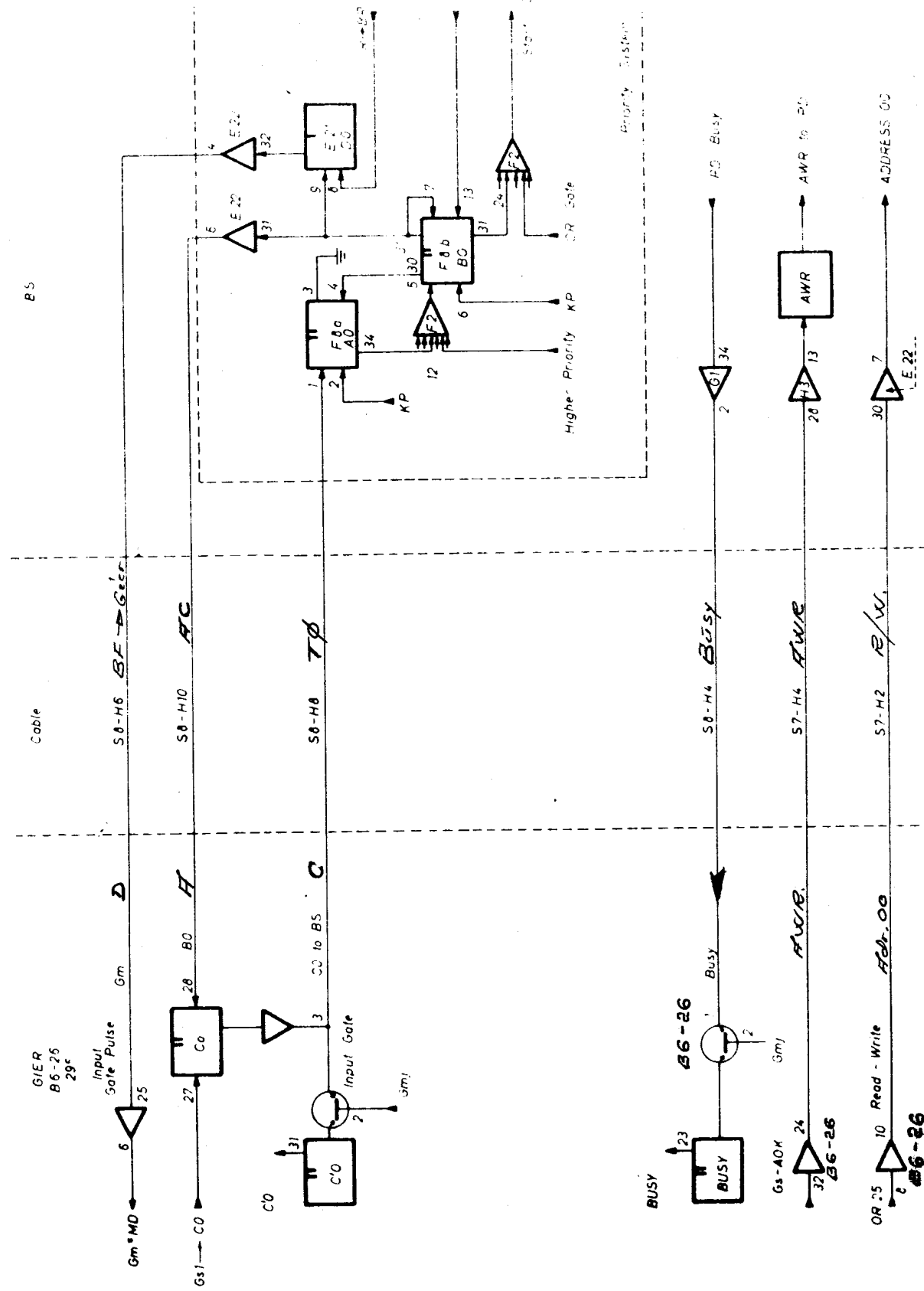
Unit: Buffer Store	Designed K.H.A.	Address Transfer.	Drawing No	
I R E G N E CENTRALEN	Approved		Drawn by G.T. 20.1.66	
	Checked 1.2.63.		Checked F.E. 19.10.67	
	Last Revision		1 Sheets	Sheet 1
			B 2	

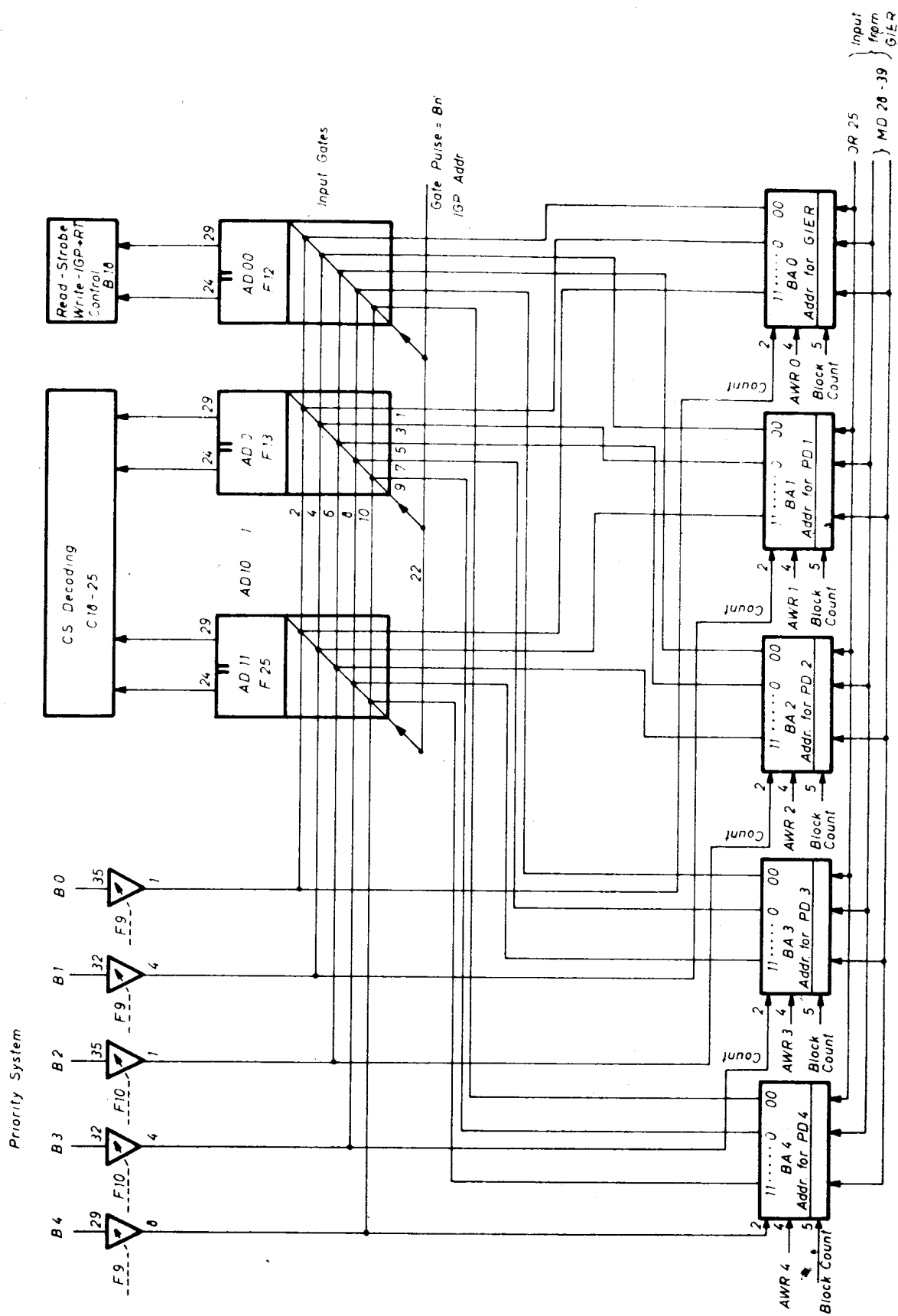
B3



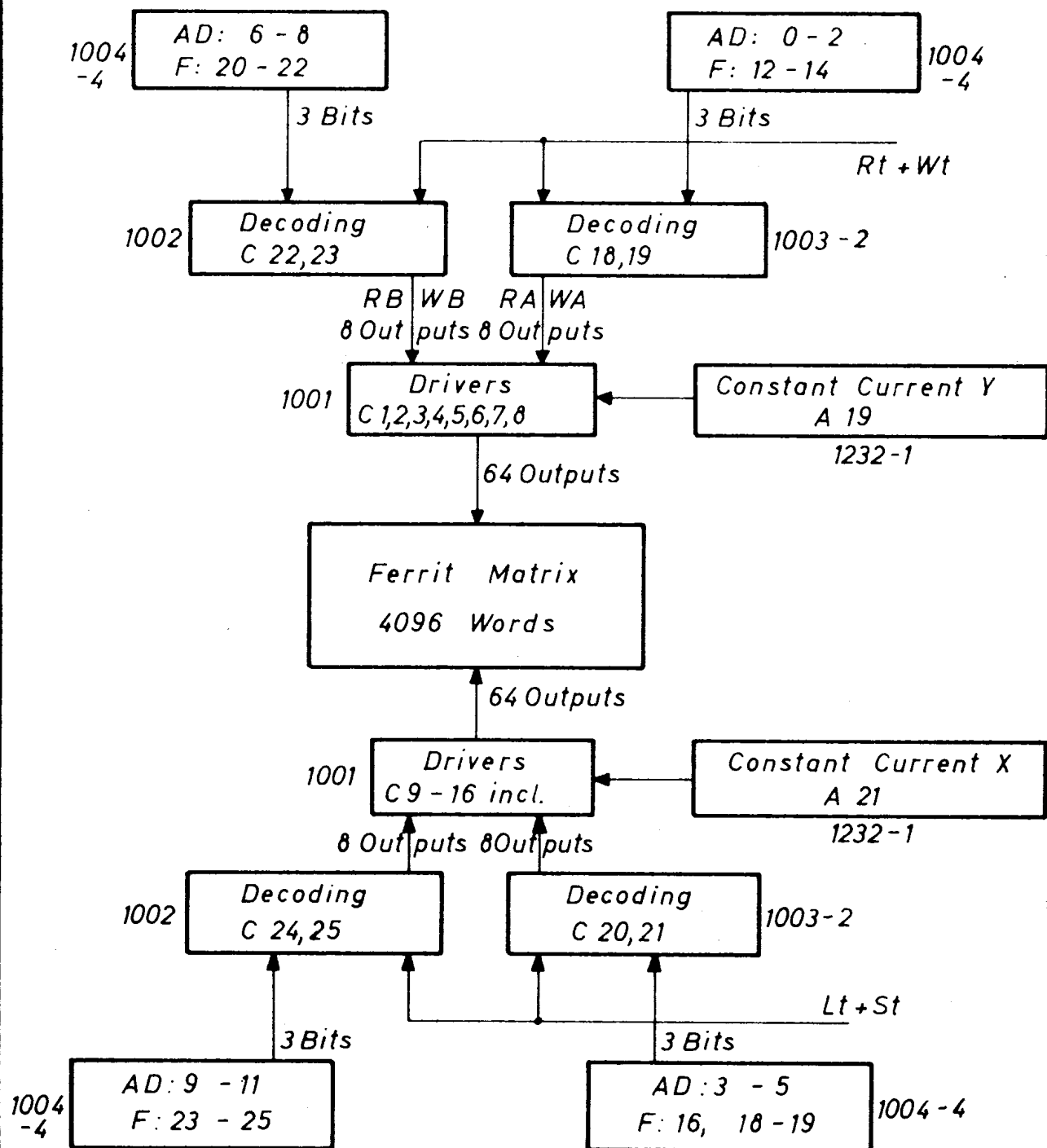
Unit: BUFFER STORE	Designed K.H.A.	Priority System	Drawing No	
	Approved		Drawn by G.T.24.2.66	
	Checked 1.2.1963		Checked FE.24.10.67	
	Last Revision		<div>1 Sheets</div> <div>Sheet 1</div>	

Unit: GIER-BS	Designed K.H.A.	SYNCHRONIZING SYSTEM	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.T. 24.2.66	
	Checked 1.2.1963		Checked F.E. 24.10.67	
	Last Revision		<div style="display: flex; justify-content: space-between;"> <u>1</u> Sheets Sheet <u>1</u> </div>	
			B5	





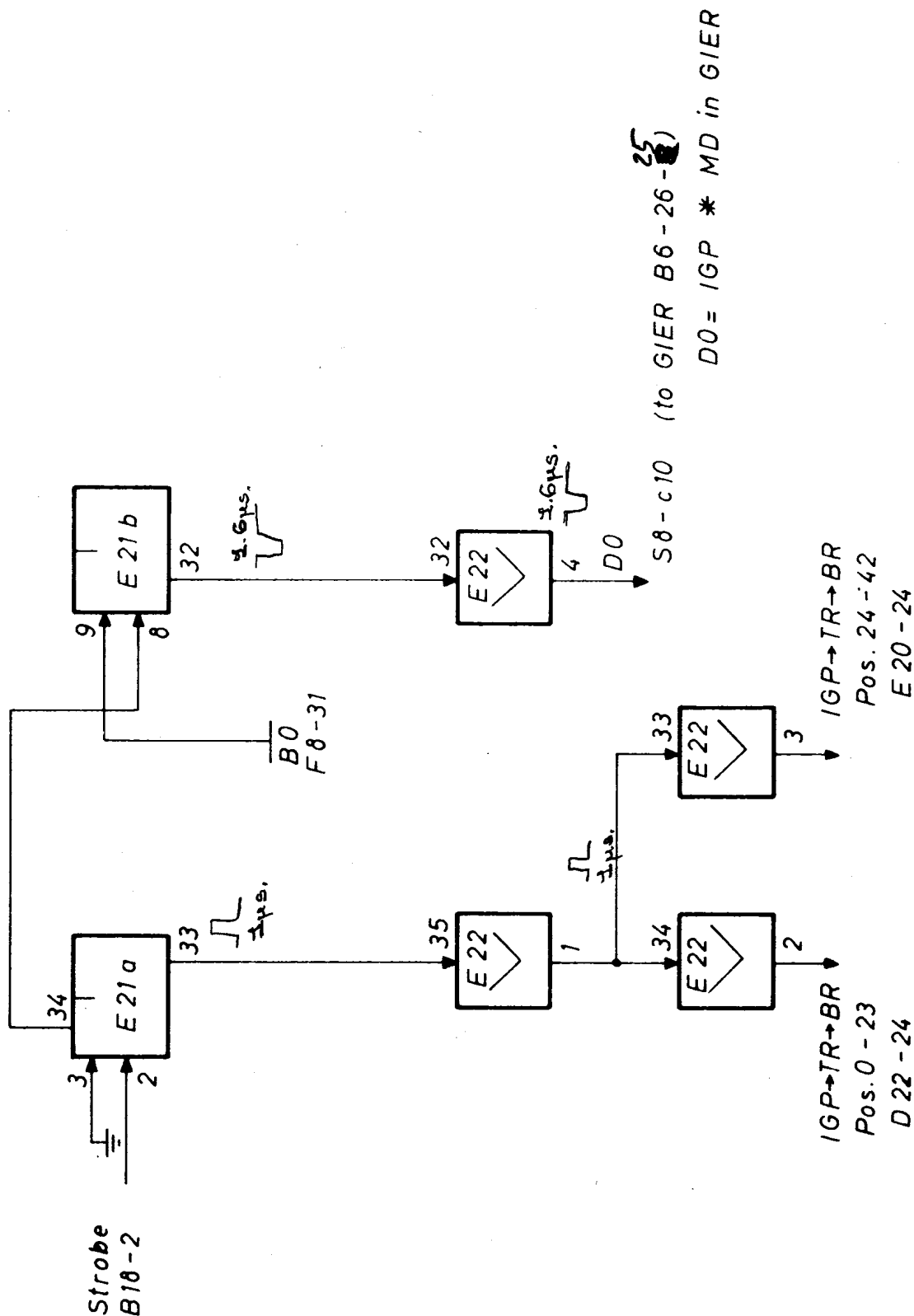
Unit BUFFER STORE	Designed K.H.A.	ADDRESS REGISTERS	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.T.24.2.66	
	Checked 1.2.1963		Checked FE. 24.10.67	
	Last Revision		1 Sheets Sheet 1	
			B6	

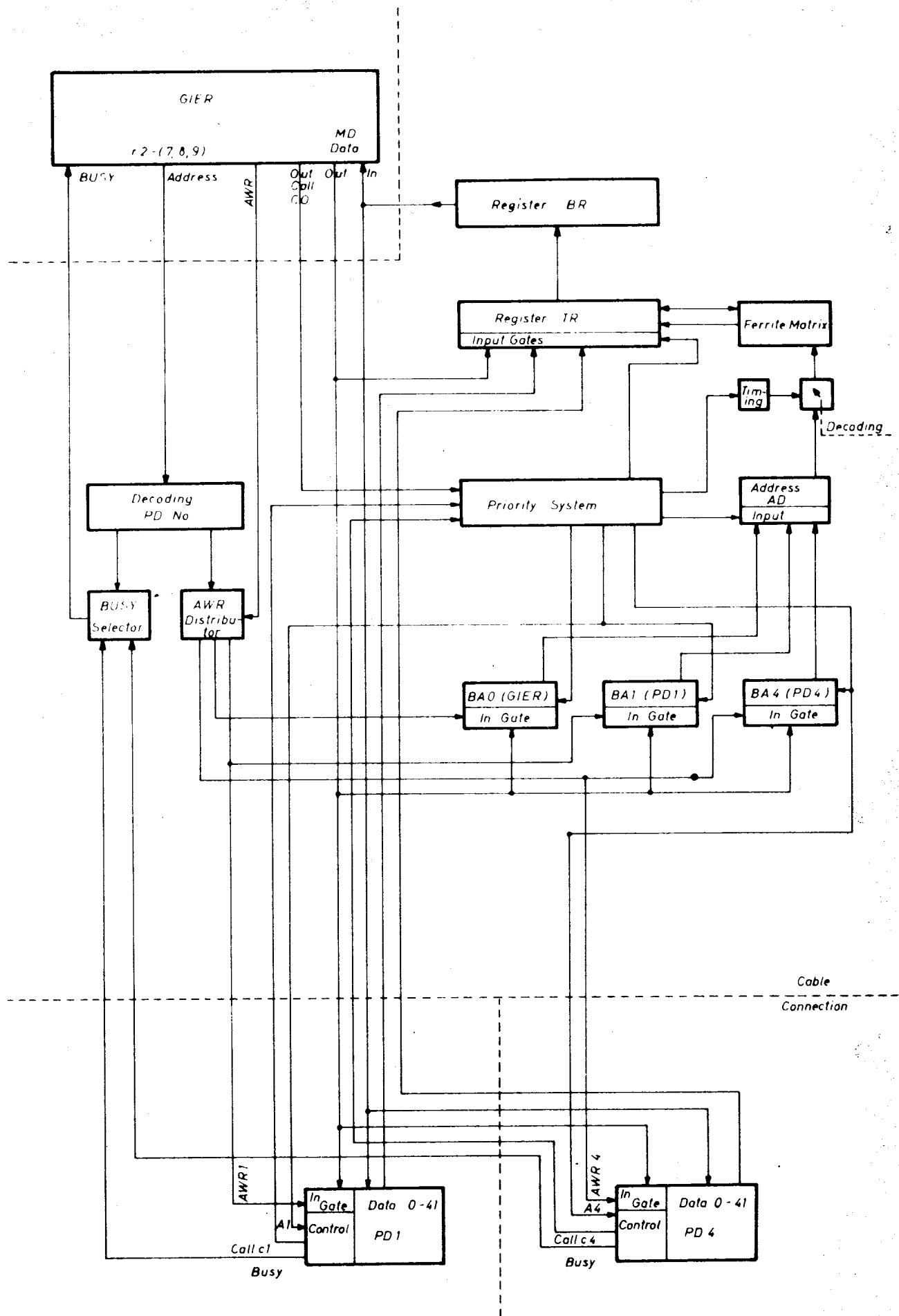



Unit: Buffer store	Designed K. H. A.	Aurus Decoding and FL Drive	Drawing No
REGNE CENTRALEN	Approved		Drawn by G. T. 2.2.66.
	Checked 1.2.66.		Checked F. E. 19.10.67
	Last Revision		1 Sheets Sheet 1
			B 7

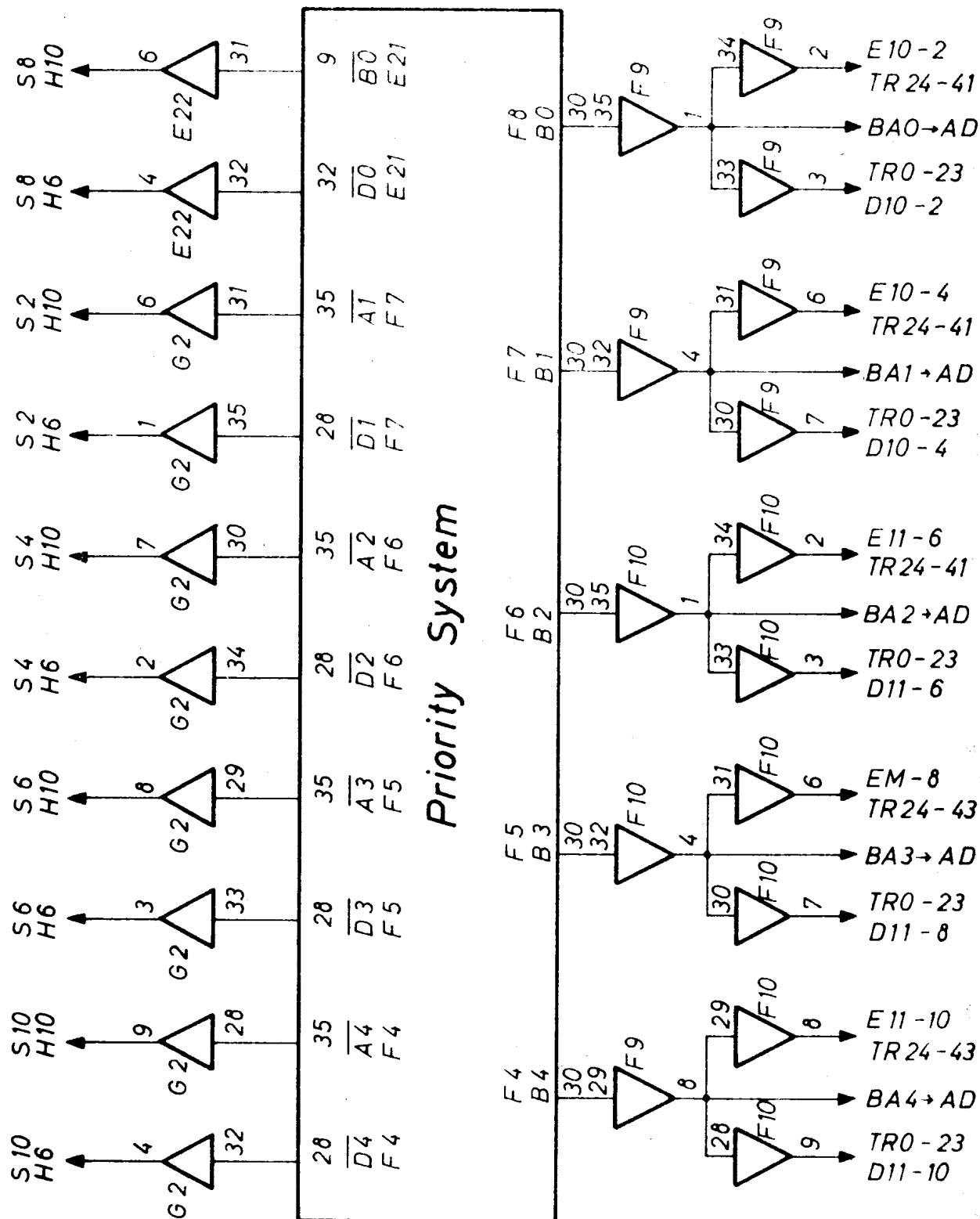
B8

REGNE CENTRALEN	Unit: Buffer Store	Designed K.H.A.	IGP-TR-BR and DO	Drawing No	
	Approved	Checked 1.2.63		Drawn by G.Y. 2.2.66	
	Last Revision			Checked F.E. 19.10.67	
				1 Sheets	Sheet 1
					B 9



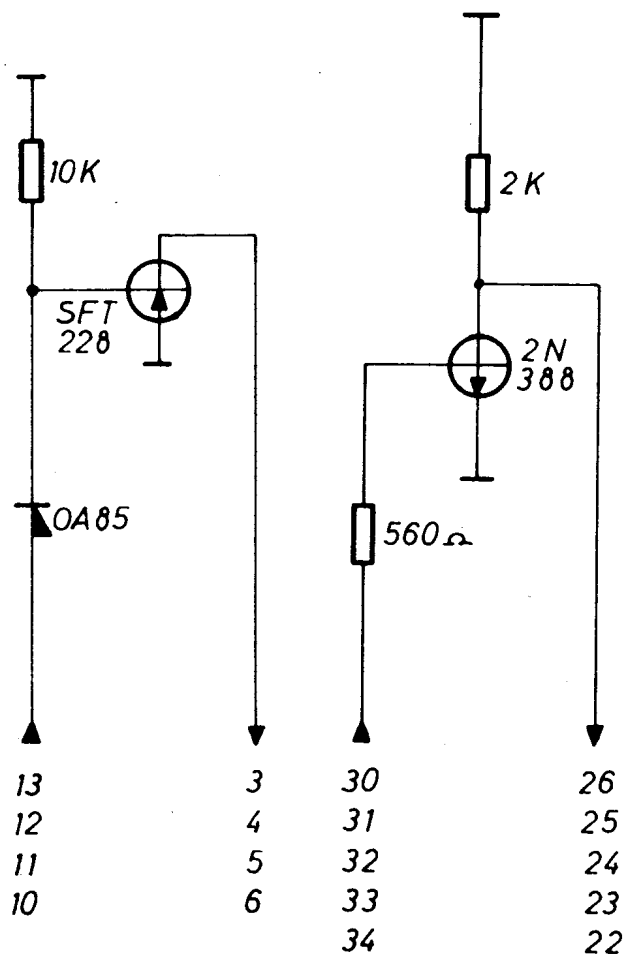


Unit BUFFER STORE	Designed K.H.A.	COMPLETE SYSTEM: BLOCK DIAGRAM	Drawing No
	Approved		Drawn by G.T.242.66.
	Checked 1.2.1963		Checked F.E. 20.10.62
	Last Revision		1 Sheets Sheet 1
			B10



Unit: Buffer store	Designed K. 1. 1.	Amplifiers Co. Priority system	Drawing No. _____	
IRENE CENTRALEN	Approved		Drawn by G. L. 1. 1. 1.	
	Checked 1. 2. 63.		Checked F. E. 19. 10. 67	
	Last Revision		1 Sheets	Sheet 1
			B 11	

5 Circuits



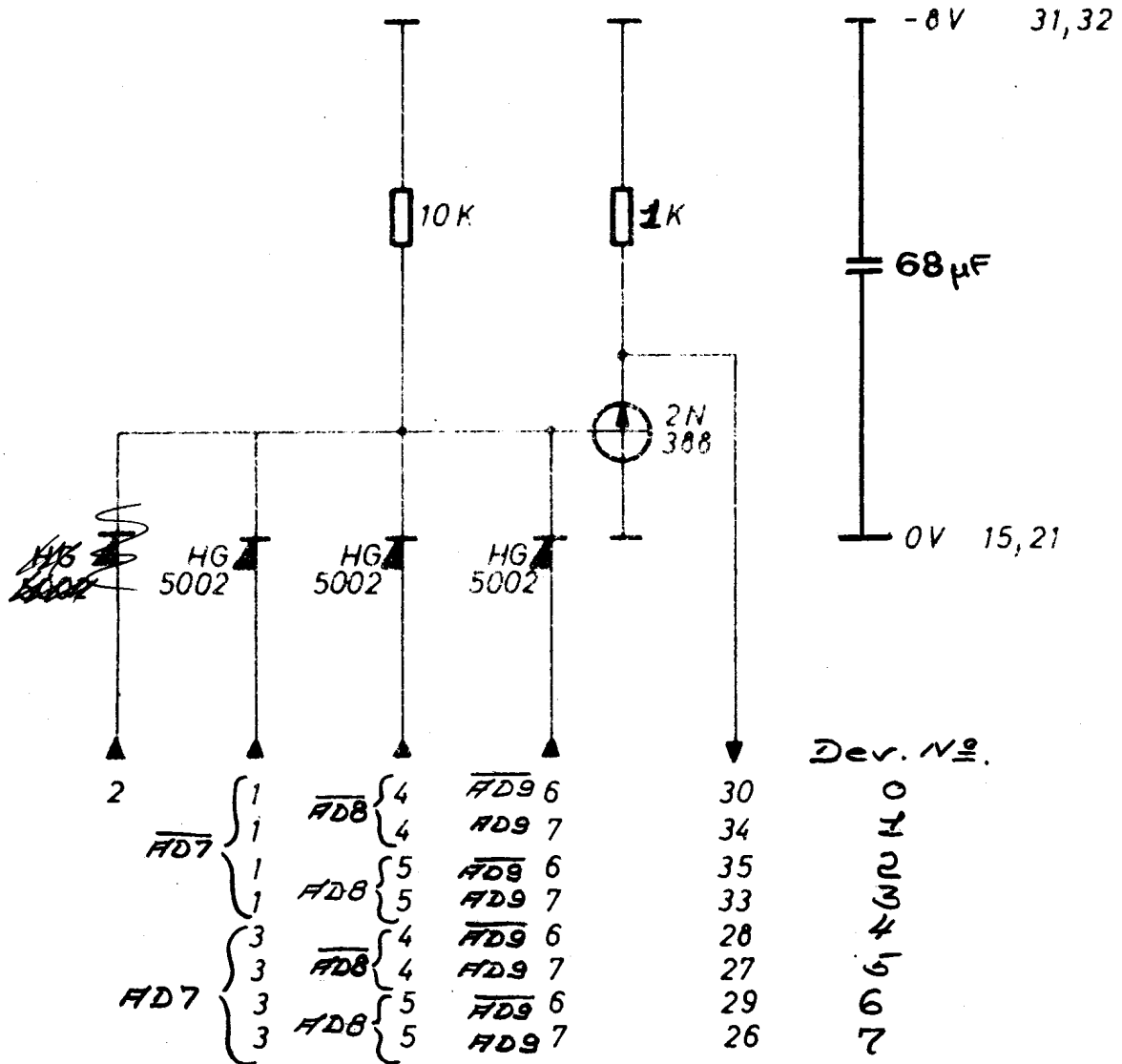
— +8V 29
— -8V 8

— 0V 7

— -1.6V 27

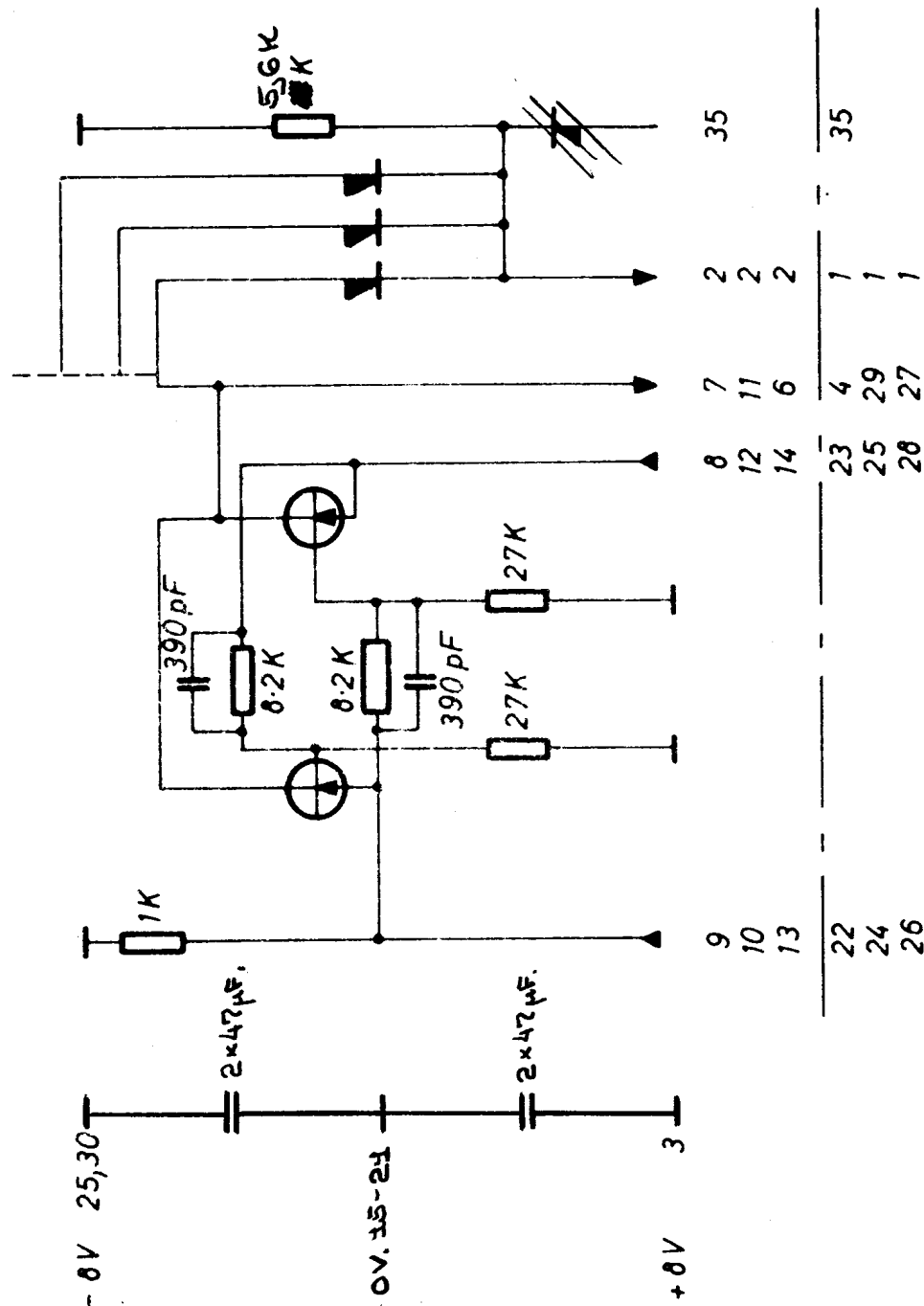
Unit: Buffer Store	Designed K.H.A.	Amplifier for Block Count	Drawing No
	Approved		Drawn by E.T.31.1. 66
	Checked 1.2.63-		Checked F.E.20.07
	Last Revision		1 Sheets Sheet 1
			H 5 200-30

6 Circuits.



Unit Buffer/DFA200	Designed K.H.A.	Decoding	Drawing No	
	Approved		Drawn by S.Y. 28.5.68	
	Checked 1.2.63.		Checked T.R. 18.2.68	
	Last Revision 26.3.68		1 Sheets	Sheet 1
			H 1	203-7

2x3 Circuits.



Unit Buffer/DFA20

IRFEGNE
CENTRALEN

Designed K. H. A.

Approved

Checked 1.2.63.

Last Revision 26.3.68

Exclusiv or Gate

Drawing No

Drawn by G. Y. 28.1.68

Checked / K. 15.3.1968

1 Sheets

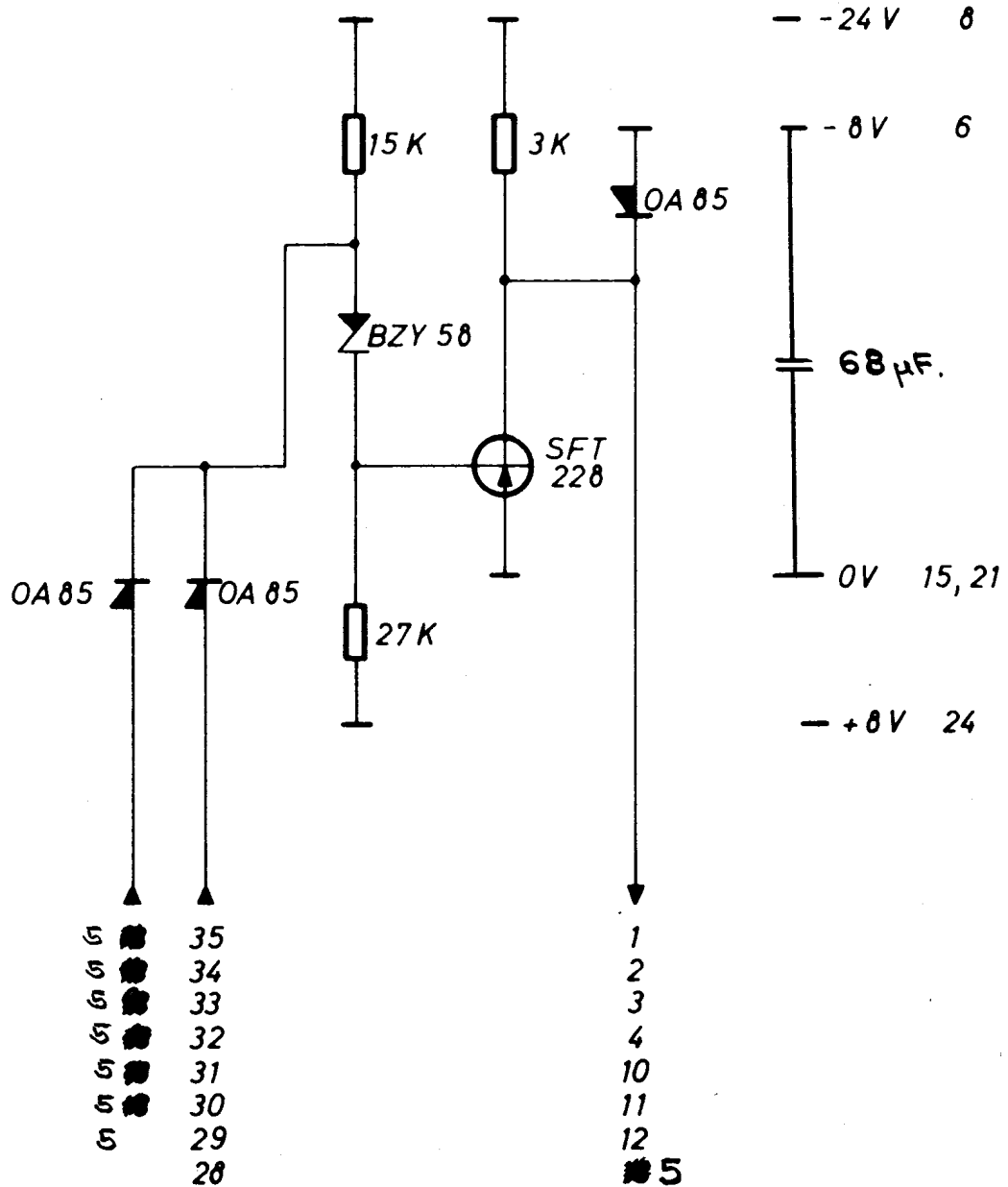
Sheet 1

M7-HA

291-14

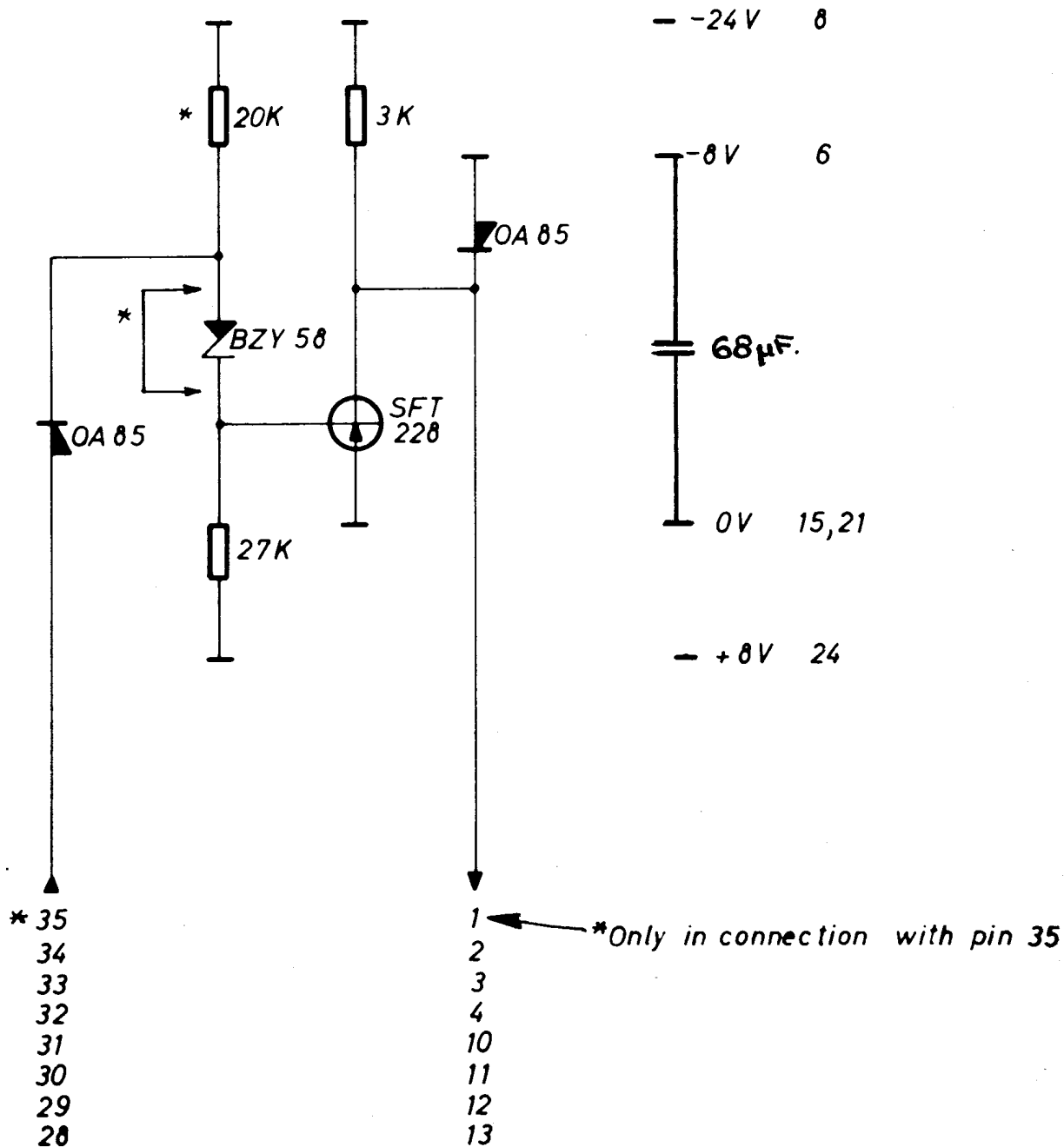
Unmarked Diodes: OA05
Transistors: SFT 220

8 Circuits.

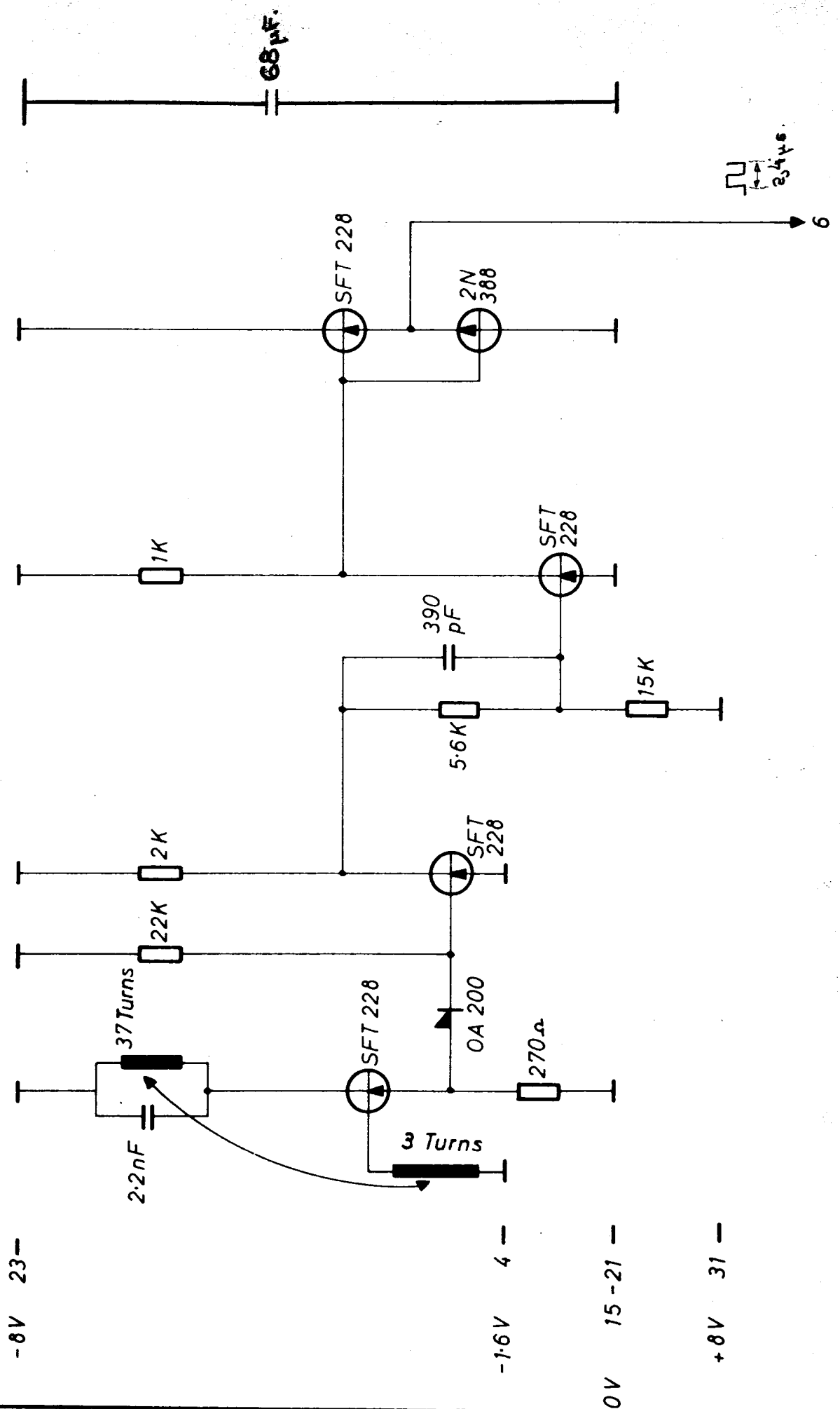


Unit Buffer/DFA20	Designed K.H.A.	Gate with Inverter Amplifier	Drawing No	
	Approved		Drawn by	
	Checked 1.2.63.		Checked	
	Last Revision 26-3-68		1 Sheets	Sheet 1
			W 3	302-9

8 Circuits.

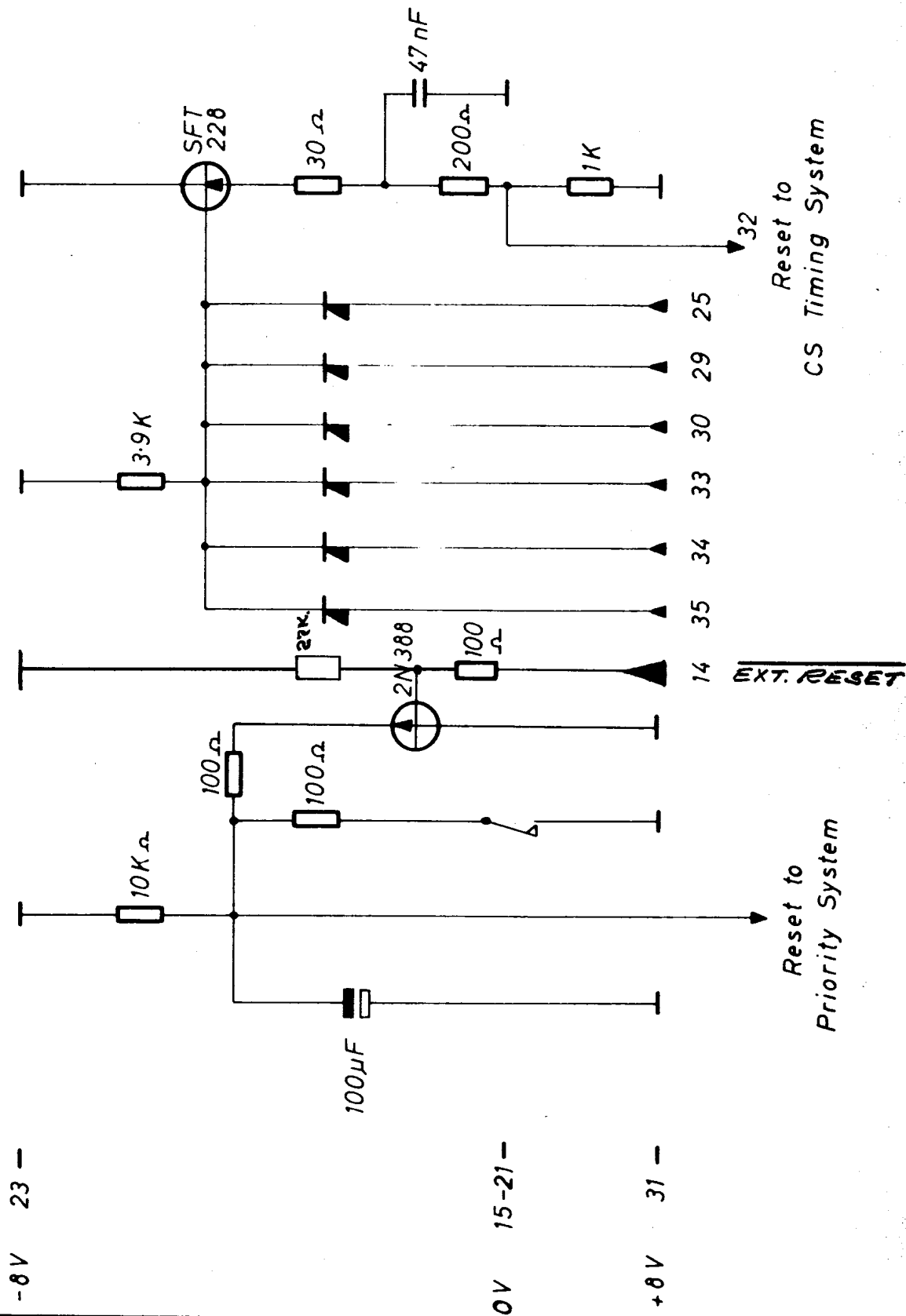


Unit Buffer/DFA200	Designed K.H.A.	Inverter Amplifier	Drawing No
	Approved		Drawn by G.T. 28.1.66
	Checked 1.2.63		Checked F.E. 28.1.67
	Last Revision 26.3.68		1 Sheets Sheet 1 61 309-10



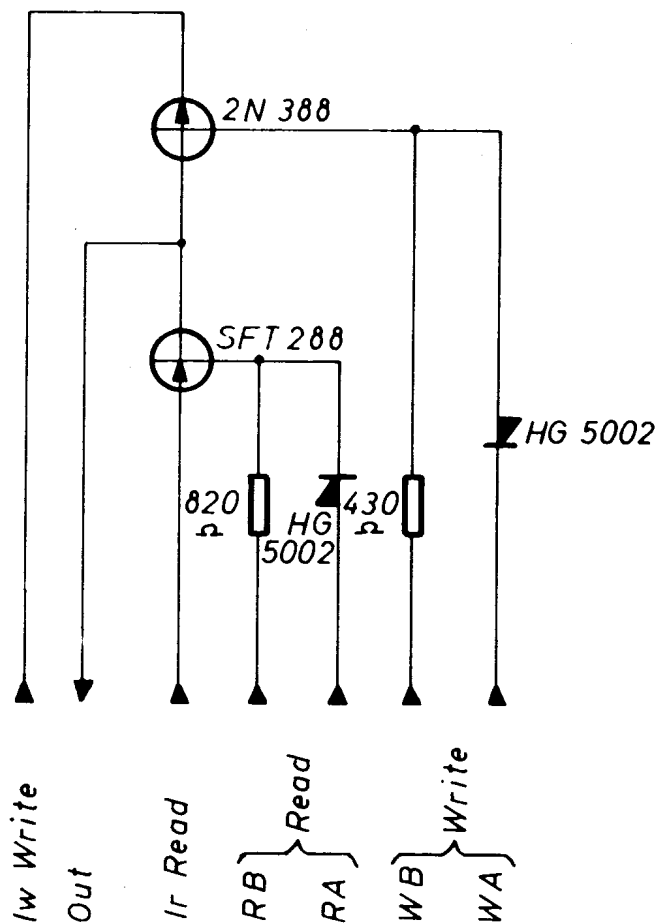
Unit: Buffer Store	Designed K.H.A.	Clock Generator and Reset	Drawing No	
	Approved		Drawn by G.T. 26.1.66	
	Checked 1.2.63.		Checked F.E. 20.10.67	
	Last Revision		2 Sheets	Sheet 1
			B 24	10000-16
			partial	

Unmarked Diodes: OA95



REGNE CENTRALEN	Unit: Buffer Store	Designed K. H. A.	Clock Generator and Reset		Drawing No	
	Approved				Drawn by G.T. 26.1.66	
	Checked 1.2.63.				Checked F.E. 20.10.67	
	Last Revision				2 Sheets	Sheet 2
					B 24	1000A-18 partial

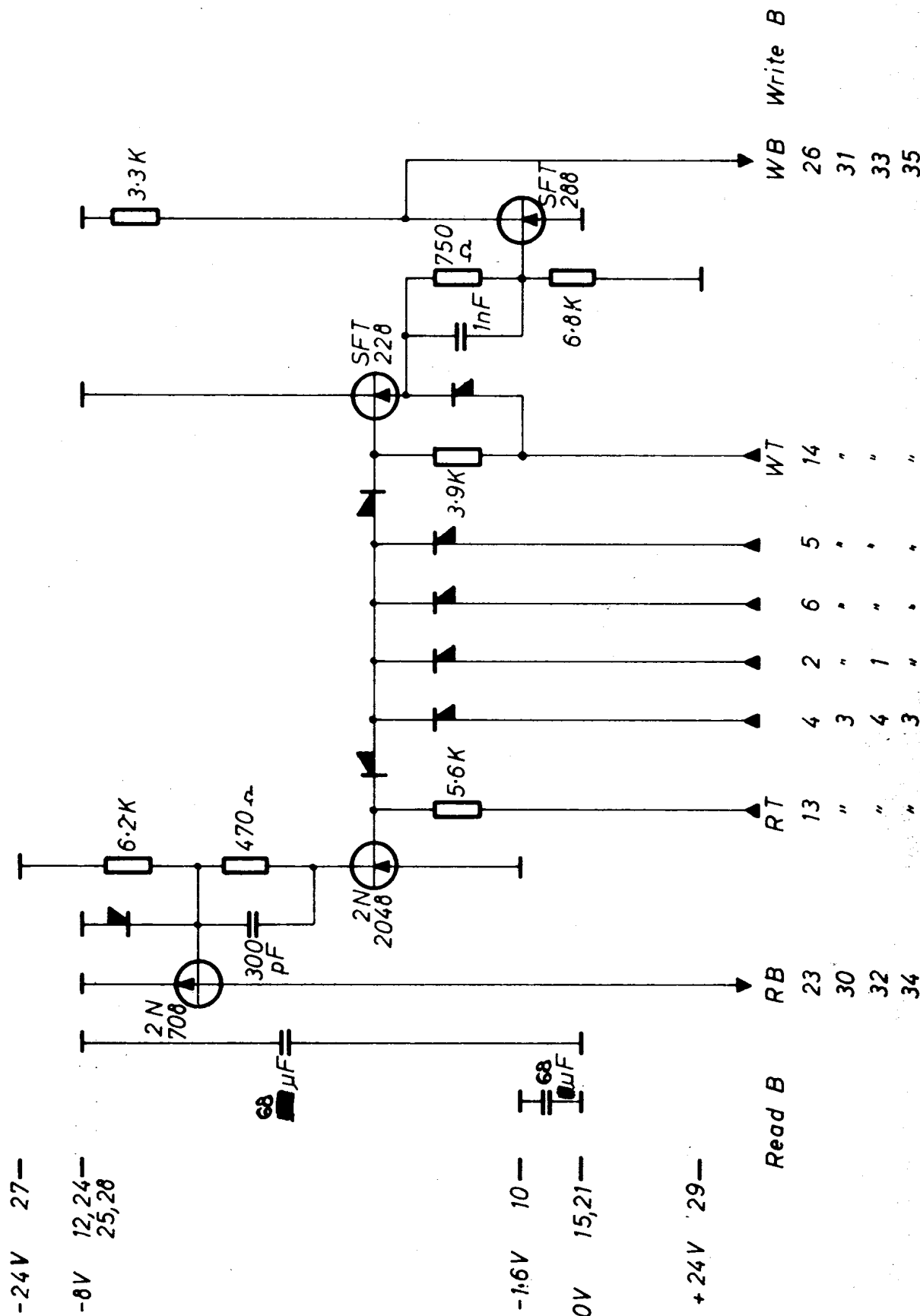
8 Circuits

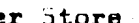


No:							
0	10-11	35	12-13	14	27	9	1
1	"	34	"	"	26	"	2
2	"	33	"	"	25	"	3
3	"	32	"	"	24	"	4
4	"	31	"	"	23	"	5
5	"	30	"	"	22	"	6
6	"	29	"	"	21	"	7
7	"	28	"	"	15	"	8

Unit: Buffer store	Designed K.H.A.	Ferrit Matrix Drivers	Drawing No	
REGNE CENTRALEN	Approved		Drawn by G.T. 31.1.64	
	Checked 1.2.63.		Checked F.E. 20-10-67	
	Last Revision		1 Sheets	Sheet 1
		G1-16 1001		

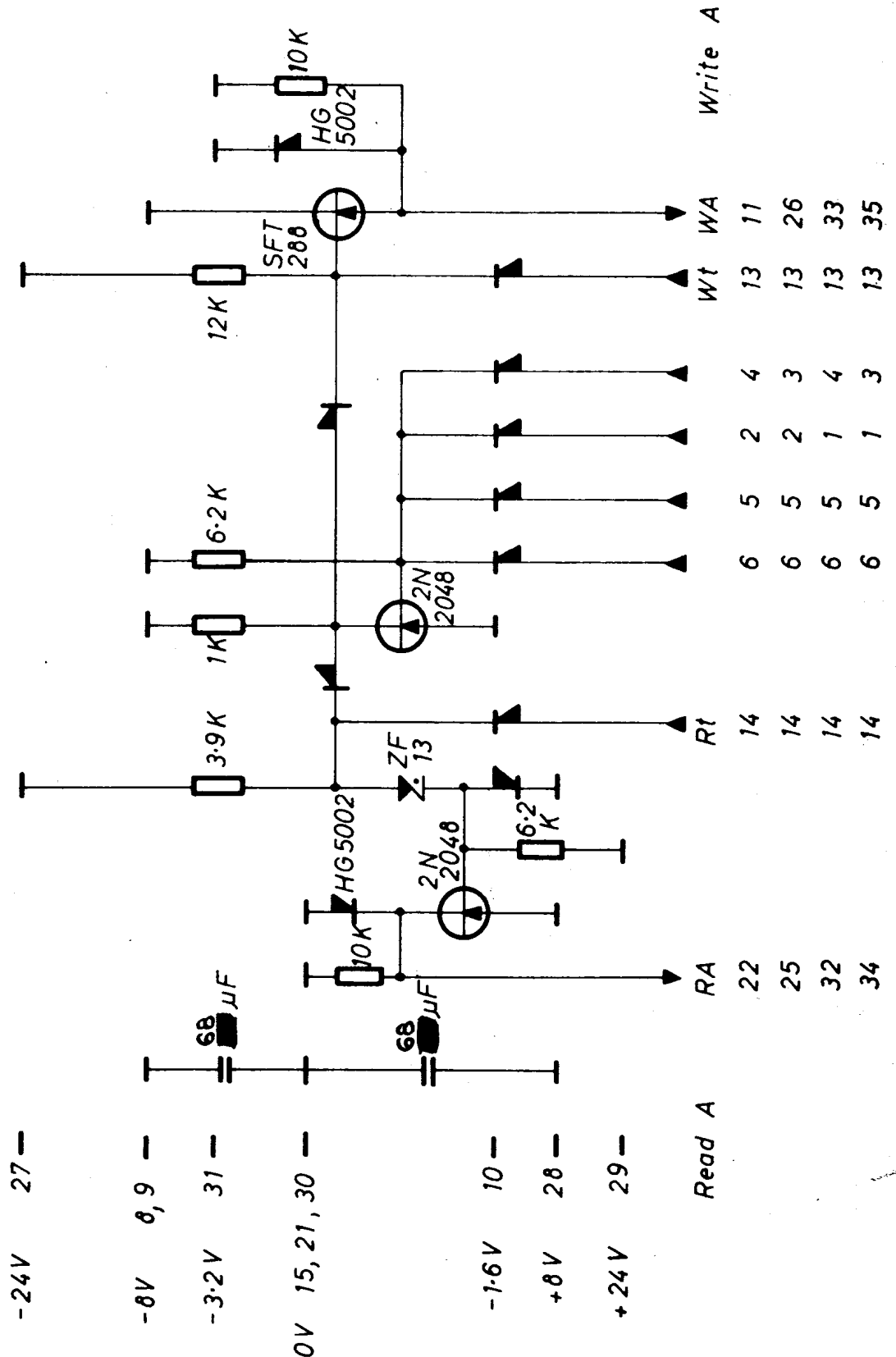
4 Circuits



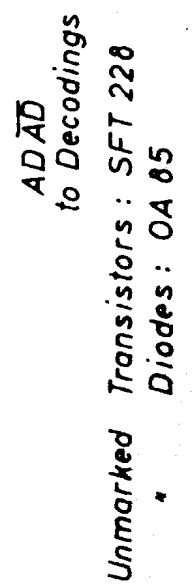
Unit: Buffer Store	Designed K.H.A.	Gate for Base Current for Drivers	Drawing No
	Approved		Drawn by G.T. 1.2.66.
	Checked 1.2.63.		Checked F.E. 20-10-67
	Last Revision		1 Sheets Sheet 1
			C22-25 1002

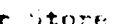
4 Circuits.

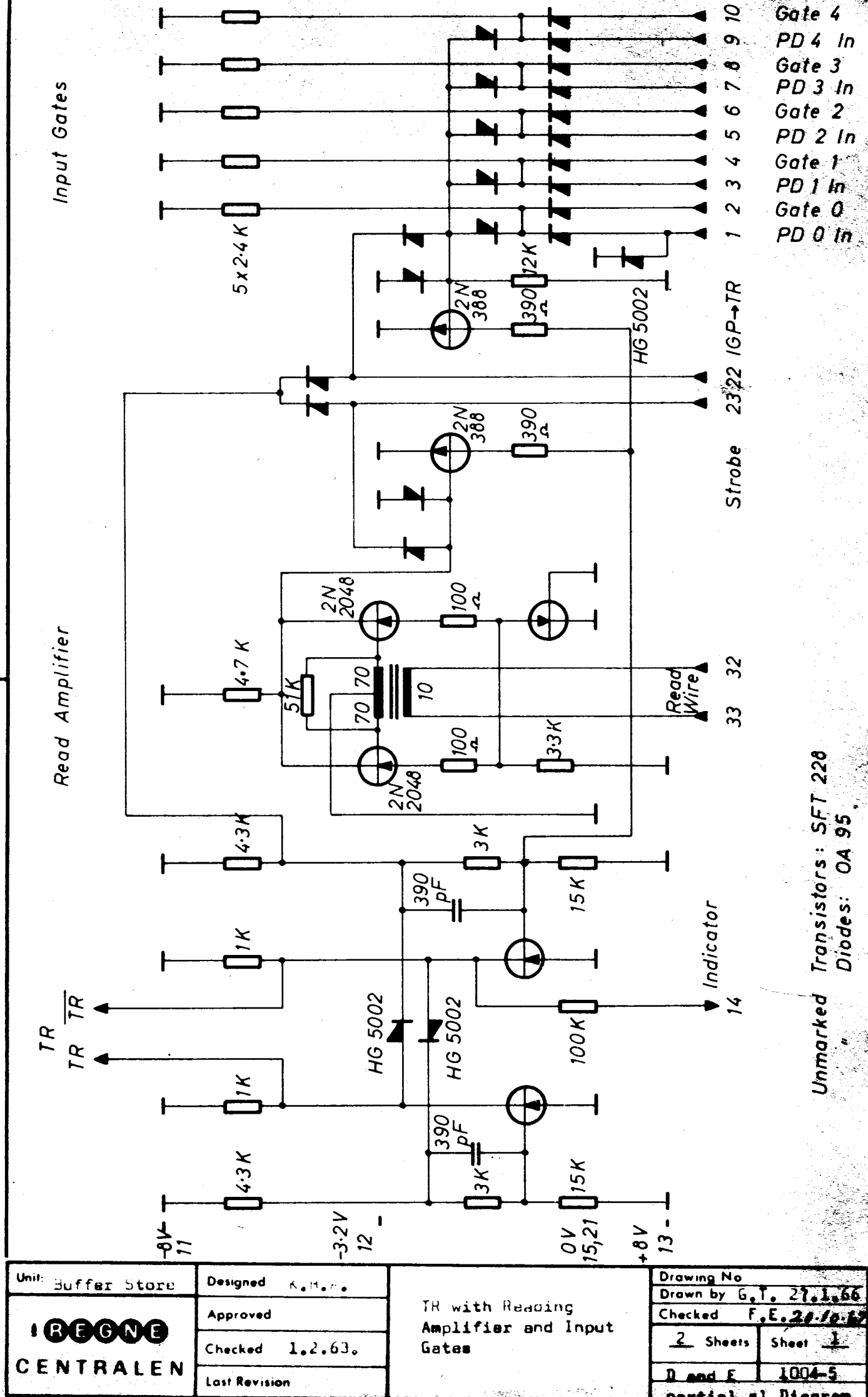
Unmarked Diodes: OA 85



IREGNE CENTRALEN	Unit: Buffer Store	Designed K.H.A.	Decoding for Blocking of Base Current for Drivers		Drawing No	
	Approved				Drawn by G.T. 28.1.66	
	Checked 1.2.63.				Checked F.E. 20/0.62	
	Last Revision				1 Sheets	Sheet 1
					C 18-21	1003-2



Unit Buffer Store	Designed F. E. 1.2.63.	Address Register	Drawing No
	Approved		Drawn by G. I. 3.2.66
	Checked 1.2.63.		Checked F. E. 20-10-67
	Last Revision		<div> <div>— Sheets</div> <div>Sheet —</div> </div> <div> <div>F12-25</div> <div>1004-4</div> </div>



Unit: Buffer Store

IREGNE
CENTRALEN

Designed K.H.F.

Approved

Checked 1.2.63.

Last Revision

TR with Reading
Amplifier and Input
Gates

Drawing No

Drawn by G.T. 27.1.66

Checked F.E. 20.10.67

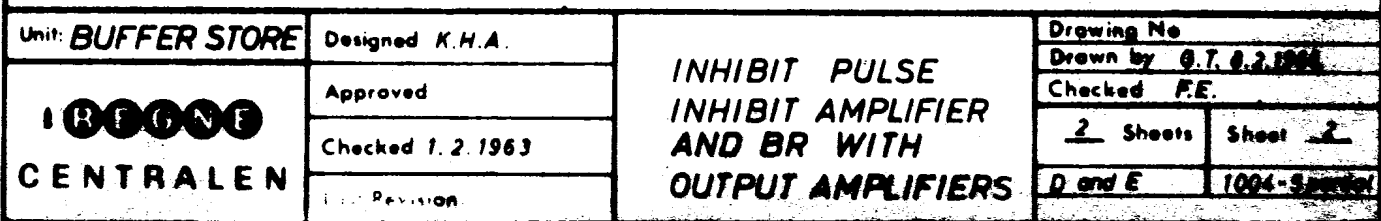
2 Sheets

Sheet 1

D and E

1004-5

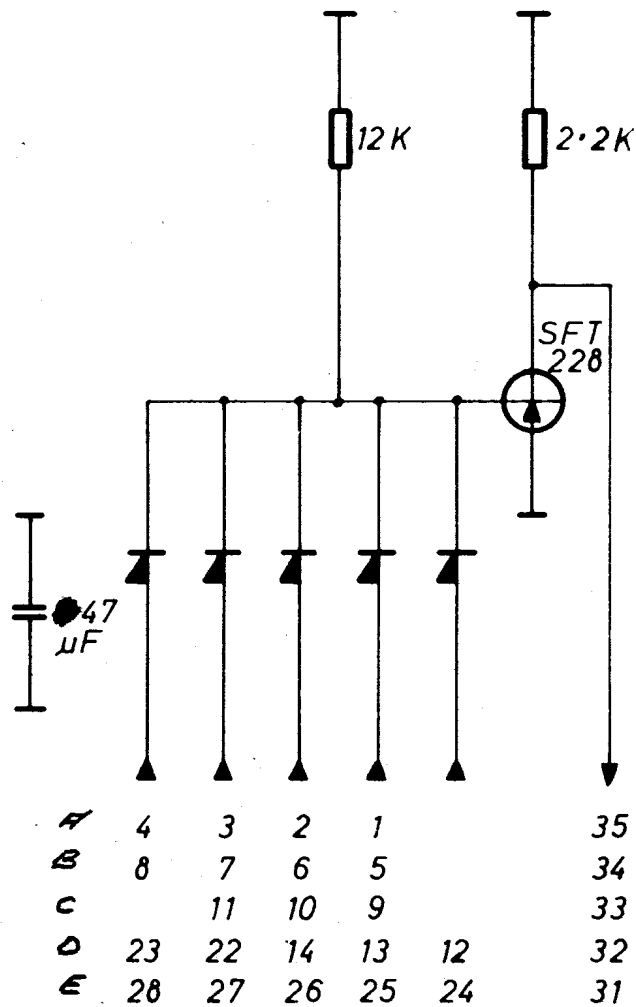
partial al Diagram



-8V 30 -


÷ 3.2V,
29 -

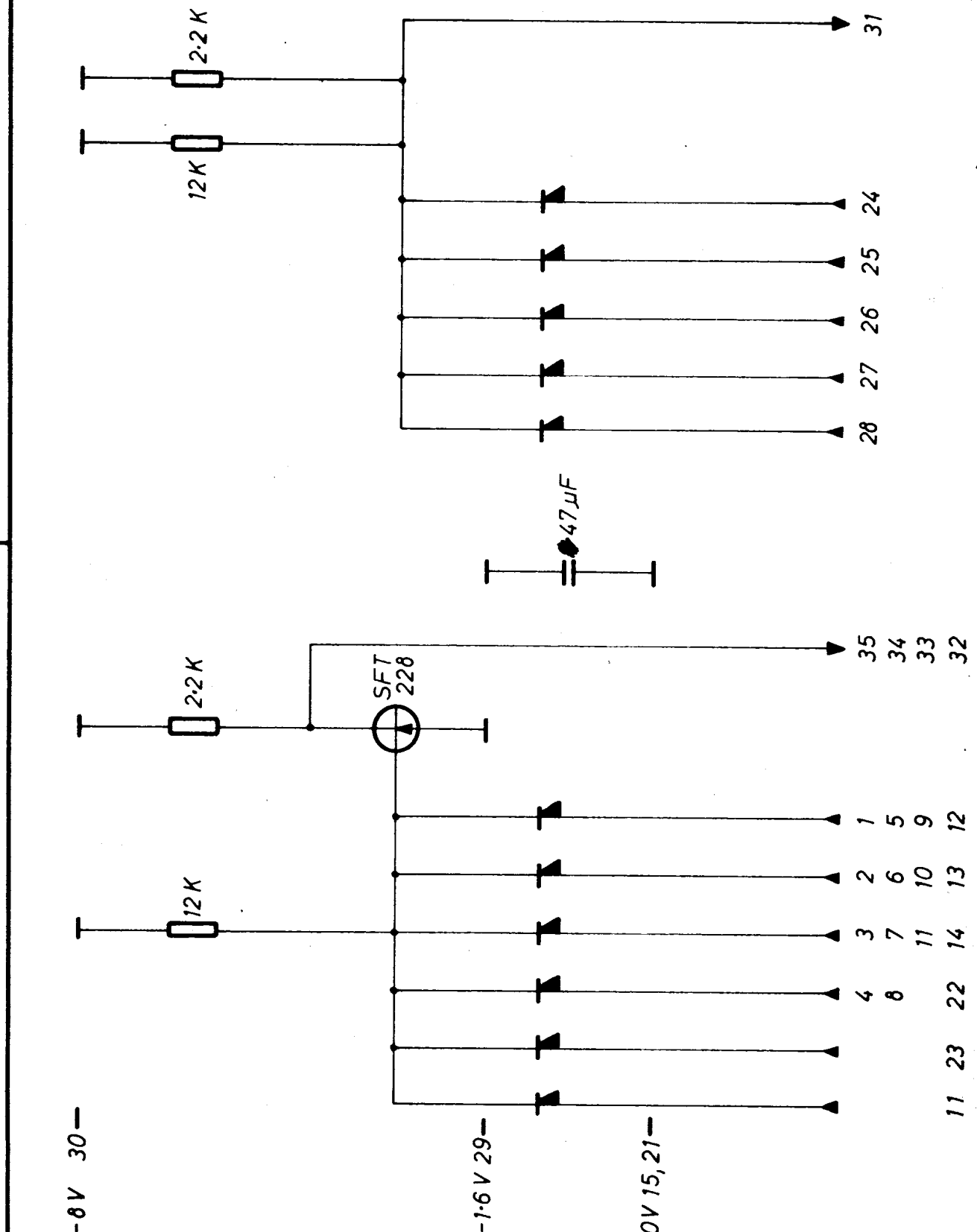
0V 15-21 -



Unmarked Diodes: OA 85

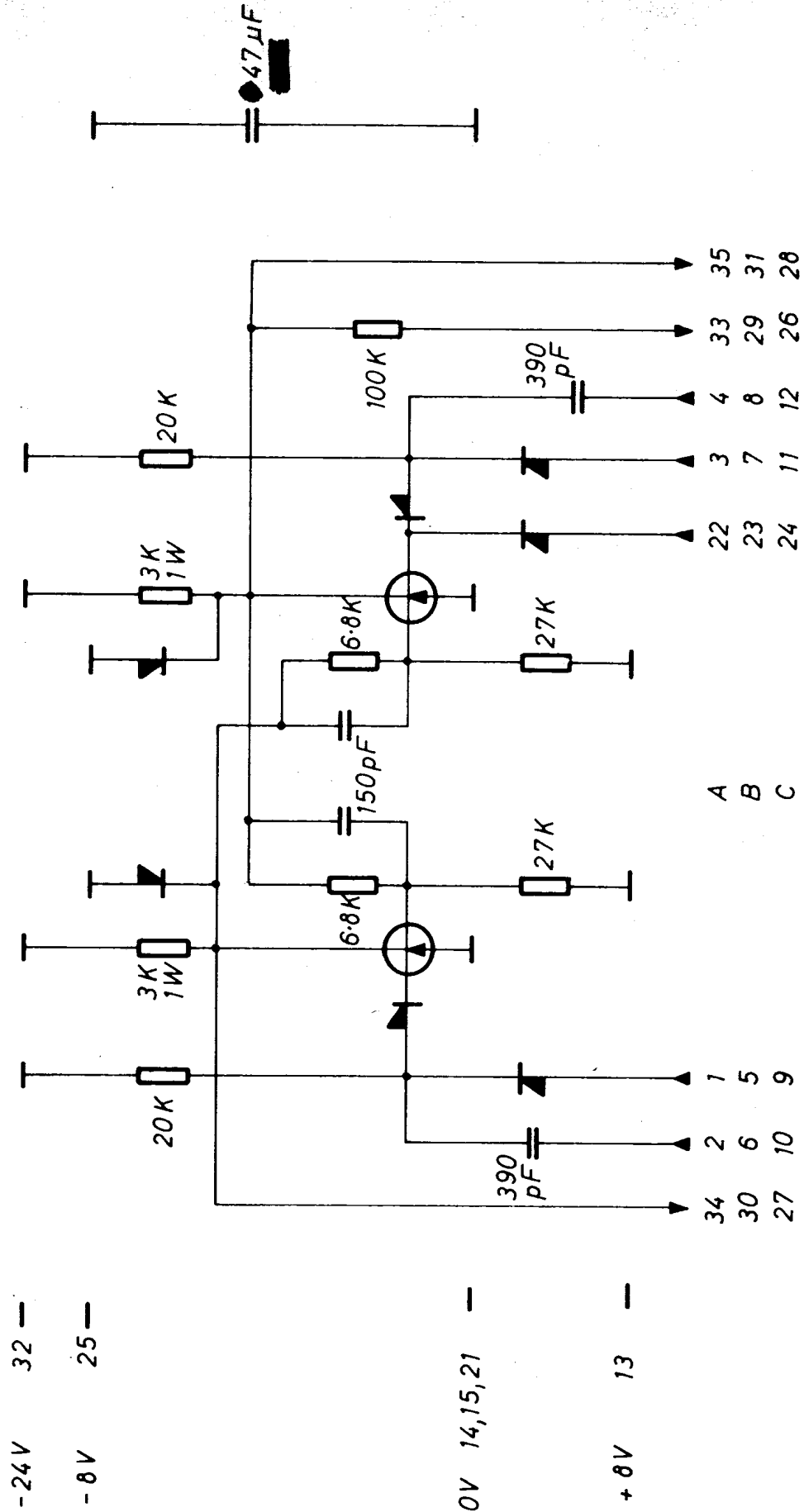
Unit: Buffer Store REGNE CENTRALEN	Designed K.H.A.	Gate with Inverter	Drawing No	
	Approved		Drawn by E.T. 28.1.63	
	Checked 1.2.63.		Checked F.E. 28.10.63	
	Last Revision		1 Sheets	Sheet 1
			H 2	1008

Unit: Buffer Store 	Designed * K.H.A.	Gate with Inverter	Drawing No	
	Approved		Drawn by G.T. 28.1.66	
	Checked 1.2.63.		Checked F.E. 20.10.67	
	Last Revision		1 Sheets	Sheet 1
			F 2	1005-1



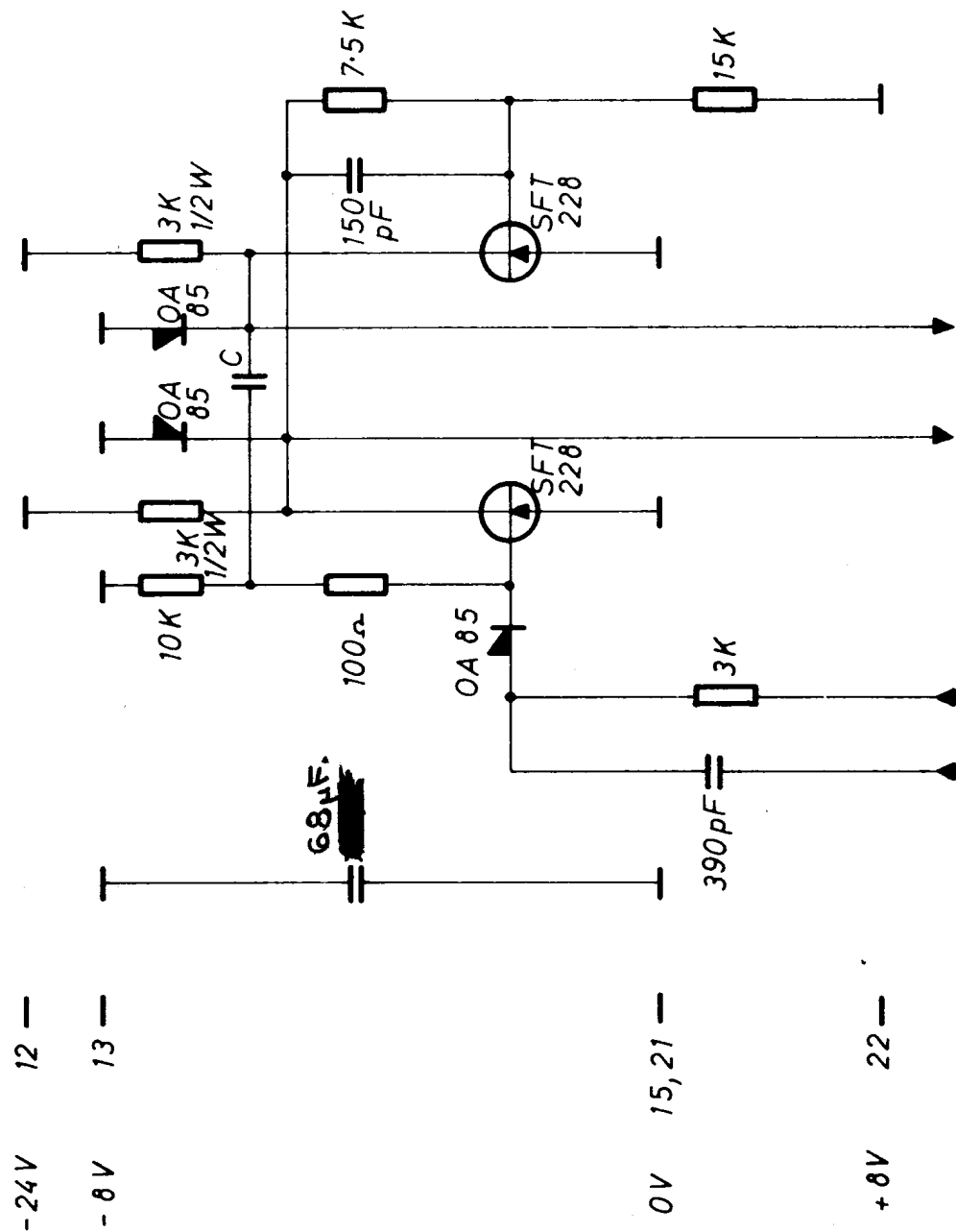
Unmarked Diodes: OA 85

3 Circuits



Unmarked Transistors: SFT 228
Diodes: OA 95

Unit: Buffer Store	Designed K.H.A.	Flip-Flop	Drawing No
! REGNE CENTRALEN	Approved		Drawn by G.T. 31.1.66
	Checked 1.2.63.		Checked F.E. 20.10.67
	Last Revision		1 Sheets Sheet 1
			F 3- F 8 1006A-1



Read 2 3 C=200pF 34 33 End Read
Write 8 9 C=150pF 32 31 End Write

Unit: Buffer Store

Designed K.H.

Monostable Flip-Flop
Used in FL Timing

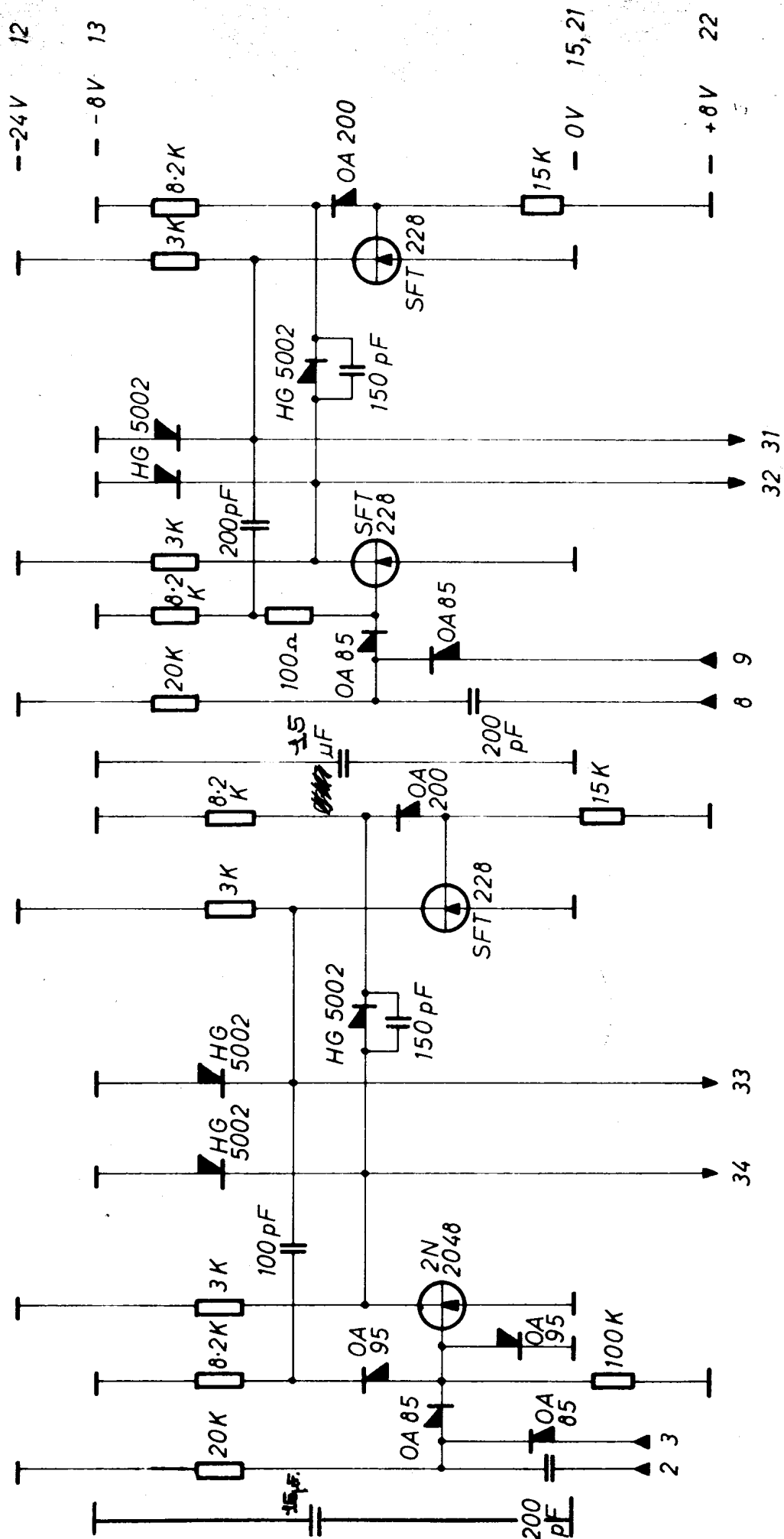
Drawing No
Drawn by G.T. 31.1.66
Checked F.E. 20.10.67
1 Sheets Sheet 1
B 20 1007-2

REGNE
CENTRALEN

Approved

Checked 1.2.63.

Last Revision



Unit: Buffer Store

Designed K.H.A.

IGP -- TR -- BR and
DO -- GIER

Drawing No

Drawn by G.T. 4.2.66.

Checked F.E. 20.10.67

REGNE
CENTRALEN

Approved

Checked 1.2.63.

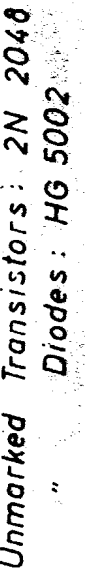
Last Revision

1 Sheets

Sheet 1

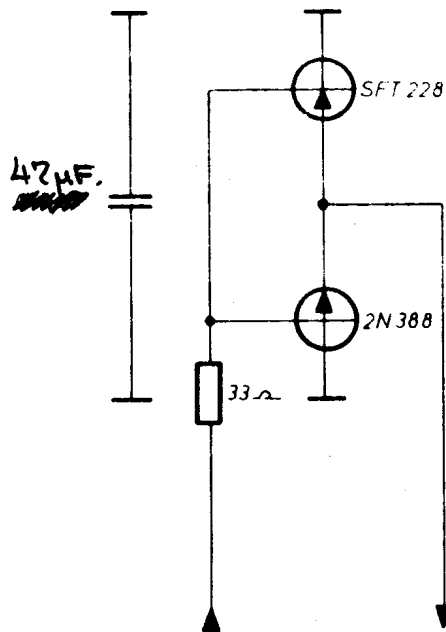
E 21

1007-3



Unmarked Transistors: 2N 2048
" Diodes: HG 5002

8 Circuits.



— -8V 5

— 0V 15, 21

A:	35	1
B:	34	2
C:	33	3
D:	32	4
E:	31	6
F:	30	7
G:	29	8
H:	28	9

Unit: BUFFER STORE

Designed K.H.A.

REGNE
CENTRALEN

Approved

Checked 1. 2. 63.

Last Revision

AMPLIFIERS.

Drawing No

Drawn by G.T. 12. 7. 67.

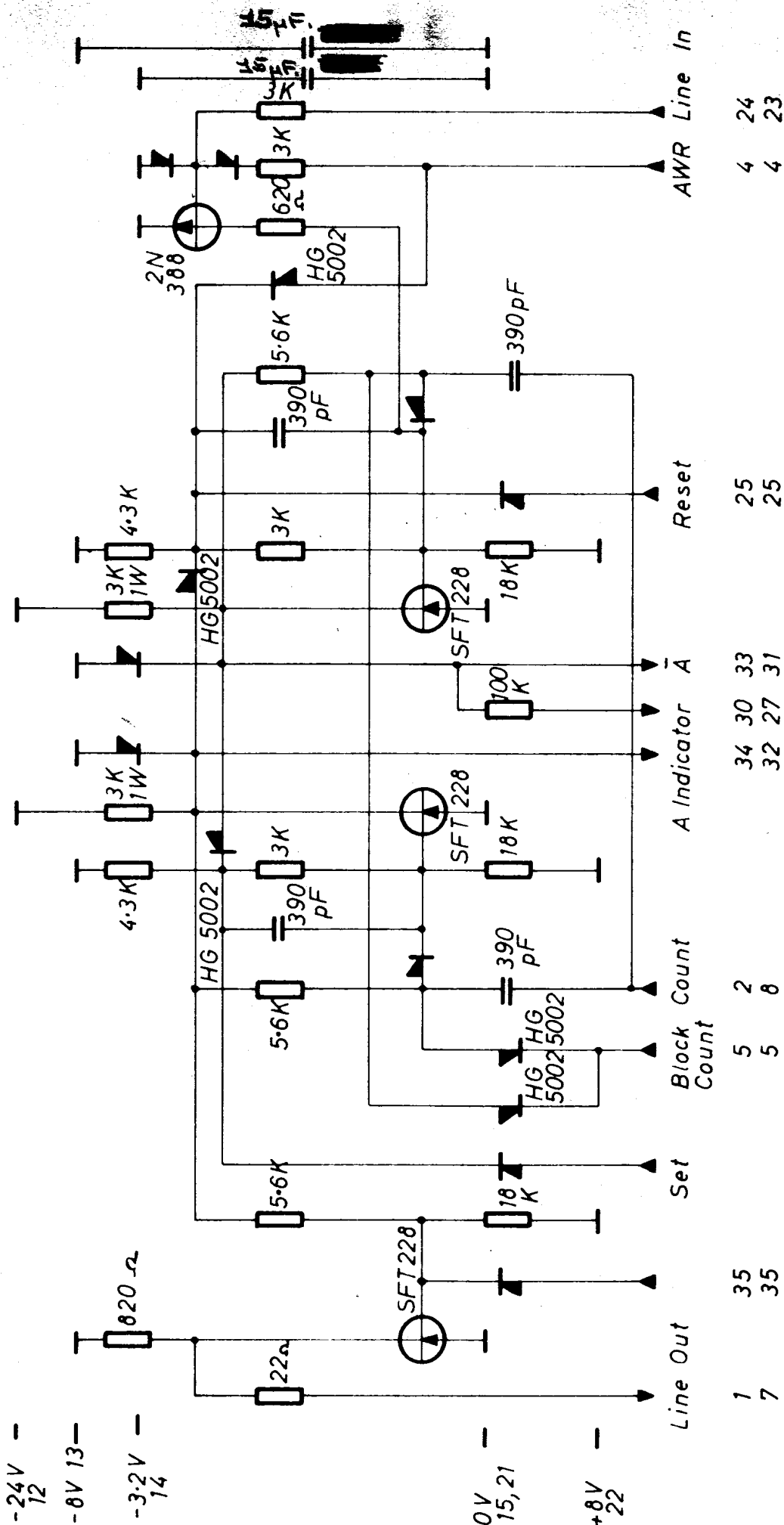
Checked F.E. 20. 10. 67

1 Sheets

Sheet 1

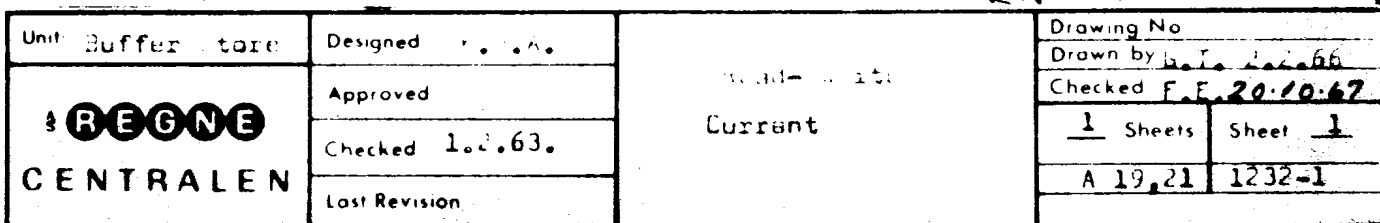
B, E, F, G, H

1008




Unmarked Diodes: OA 95


Unit Buffer Store	Designed K.H.A.	Flip-Flop with Line in and Line Out and Counting	Drawing No	
! REGNE CENTRALEN	Approved		Drawn by G.I. 4.2.66	
	Checked 1.2.63.		Checked F.E. 20.10.67	
	Last Revision		<u>1</u> Sheets	Sheet <u>1</u>
			G.H.	1017




Pin	Wired To	Wired To	Name of Signal
A3	D5-27	S3-A3	4
A5	D4-27	S3-A5	3
A7	D3-27	S3-A7	2
A9	D2-27	S3-A9	1
A11	D1-27	S3-A11	0
A13	D10-27	S3-A13	9
A15	D9-27	S3-A15	8
B2	D8-27	S3-B2	7
B4	D7-27	S3-B4	6
B6	D6-27	S3-B6	5
B8	D15-27	S3-B8	14
B10	D14-27	S3-B10	13
B12	D13-27	S3-B12	12
B14	D12-27	S3-B14	11
C1	D11-27	S3-C1	10
C3	D21-27	S3-C3	19
C5	D20-27	S3-C5	18
C7	D19-27	S3-C7	17
C9	D18-27	S3-C9	16
C11	D16-27	S3-C11	15
C13	E1-27	S3-C13	24
C15	D25-27	S3-C15	23
D2	D24-27	S3-D2	22
D4	D23-27	S3-D4	21
D6	D22-27	S3-D6	20
D8	E6-27	S3-D8	29
D10	E5-27	S3-D10	28
D12	E4-27	S3-D12	27
D14	E3-27	S3-D14	26
E1	E2-27	S3-E1	25
E3	E11-27	S3-E3	34
E5	E10-27	S3-E5	33
F111	E9-27	S3-F11	32
F13	E8-27	S3-E13	31
F15	E7-27	S3-E15	30
F2	E16-27	S3-F2	39
F4	E15-27	S3-F4	38
F12	E14-27	S3-F12	37

Unit Buffer Store	Designed K.H.A.	S 1	Drawing No	
	Approved		Drawn by L.N.L. 12.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		2 Sheets	Sheet 1


Pin	Wired To	Wired To	Name of Signal
F14	E13-27	S3-14	36
G1	E12-27	S3-G1	35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	E19-27	S3-G13	41
G15	E18-27	S3-G15	40
H2	E22-7	S3-H2	Addr. 00
H4	H4-2		AVR1
H6	H8-13		
H8	H8-10		
H10	H8-9		
H12	D10-1	S3-H12	Addr. 9
H14	D9-1	S3-H14	Addr. 8
S1	 		
S3	Chassis		0 Volts
S5		S5-S5	<u>AD1-5</u>
S7		S5-S7	<u>AD1-4</u>
S9		S5-S9	<u>AD1-3</u>
S11		S5-S11	<u>AD1-2</u>
S13	Chassis		0 Volts
S15	H5-13		
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: C-2		

Unit Buffer Store	Designed K.H.A.	S 1	Drawing No	
	Approved		Drawn by L.H.L. 12.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		<u>2</u> Sheets Sheet <u>2</u>	


Pin	Wired To	Wired To	Name of Signal
A3	D5-3		4
A5	D4-3		3
A7	D3-3		2
A9	D2-3		1
A11	D1-3		0
A13	D10-3		9
A15	D9-3		8
B2	D8-3		7
B4	D7-3		6
B6	D6-3		5
B8	D15-3		14
B10	D14-3		13
B12	D13-3		12
B14	D12-3		11
C1	D11-3		10
C3	D21-3		19
C5	D20-3		18
C7	D19-3		17
C9	D18-3		16
C11	D16-3		15
C13	E1-3		24
C15	D25-3		23
D2	D24-3		22
D4	D23-3		21
D6	D22-3		20
D8	E6-3		29
D10	E5-3		28
D12	E4-3		27
D14	E3-3		26
E1	E2-3		25
E3	E11-3		34
E5	E10-3		33
E11	E9-3		32
E13	E8-3		31
E15	F7-3		30
F2	E16-3		39
F4	E15-3		38
F12	E14-3		37

Unit Buffer Store  CENTRALEN	Designed K.H.A.	S 2	Drawing No	
	Approved		Drawn by H.L.12.5.67	
	Checked 1.2.63		Checked F.E.23.10.62	
	Last Revision		2 Sheets	Sheet 1


Pin	Wired To	Wired To	Name of Signal
F14	E13-3		36
G1	E12-3		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	E19-3		41
G15	E18-3		40
H2	Chassis		0 Volts
H4	H2-3		Busy
H6	G2-1		D
H8	F7-1		C
H10	G2-6		A
H12	D21-1	S4-H12	Addr. 19
H14	D20-1	S4-H14	Addr. 18
S1	D19-1	S4-S1	Addr. 17
S3	D18-1	S4-S3	Addr. 16
S5	D16-1	S4-S5	Addr. 15
S7	D15-1	S4-S7	Addr. 14
S9	D14-1	S4-S9	Addr. 13
S11	D13-1	S4-S11	Addr. 12
S13	D12-1	S4-S13	Addr. 11
S15	D11-1	S4-S15	Addr. 10
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U13			
U15			
	Code: G-3		

Unit Buffer Store	Designed K.H.A.	S 2	Drawing No	
	Approved		Drawn by L.N.L. 12.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		2 Sheets	Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	S1-A3	S5-A3	4
A5	S1-A5	S5-A5	3
A7	S1-A7	S5-A7	2
A9	S1-A9	S5-A9	1
A11	S1-A11	S5-A11	0
A13	S1-A13	S5-A13	9
A15	S1-A15	S5-A15	8
B2	S1-B2	S5-B2	7
B4	S1-B4	S5-B4	6
B6	S1-B6	S5-B6	5
B8	S1-B8	S5-B8	14
B10	S1-B10	S5-B10	13
B12	S1-B12	S5-B12	12
B14	S1-B14	S5-B14	11
C1	S1-C1	S5-C1	10
C3	S1-C3	S5-C3	19
C5	S1-C5	S5-C5	18
C7	S1-C7	S5-C7	17
C9	S1-C9	S5-C9	16
C11	S1-C11	S5-C11	15
C13	S1-C13	S5-C13	24
C15	S1-C15	S5-C15	23
D2	S1-D2	S5-D2	22
D4	S1-D4	S5-D4	21
D6	S1-D6	S5-D6	20
D8	S1-D8	S5-D8	29
D10	S1-D10	S5-D10	28
D12	S1-D12	S5-D12	27
D14	S1-D14	S5-D14	26
E1	S1-E1	S5-E1	25
E3	S1-E3	S5-E3	34
E5	S1-E5	S5-E5	33
E11	S1-E11	S5-E11	32
E13	S1-E13	S5-E13	31
E15	S1-E15	S5-E15	30
F2	S1-F2	S5-F2	39
F4	S1-F4	S5-F4	38
F12	S1-F12	S5-F12	37

Unit Buffer Store	Designed K.H.A.	S 3	Drawing No	
	Approved		Drawn by L.M.L. 12.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		2 Sheets	Sheet 1


Pin	Wired To	Wired To	Name of Signal
F14	S1-F14	S5-F14	36
G1	S1-G1	S5-G1	35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	S1-G13	S5-G13	41
G15	S1-G15	S5-G15	40
H2	S1-H2	S5-H2	Addr. 00
H4	H4-3		AWR2
H6	H7-20		4
H8	H7-24		2
H10	H7-22		1
H12	S1-H12	S5-H12	9
H14	S1-H14	S5-H14	8
S1	XXXXXXXXXX		XXXXXXXXXX
S3	XXXXXXXXXX		0 Volts
S5	S5-S5	S7-S5	AD5
S7	S5-S7	S7-S7	AD4
S9	S5-S9	S7-S9	AD3
S11	S5-S11	S7-S11	AD2
S13	Chassis		0 Volts
S15	H5-12		
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
Code: 6-2			

Unit Buffer Store 	Designed K.H.A.	S 3	Drawing No	
	Approved		Drawn H.N.L.12.5.67	
	Checked 1.2.63		Checked F.E.23-10-67	
	Last Revision		2 Sheets	Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	D5-5		4
A5	D4-5		3
A7	D3-5		2
A9	D2-5		1
A11	D1-5		0
A13	D10-5		9
A15	D9-5		8
B2	D8-5		7
B4	D7-5		6
B6	D6-5		5
B8	D15-5		14
B10	D14-5		13
B12	D13-5		12
B14	D12-5		11
C1	D11-5		10
C3	D21-5		19
C5	D20-5		18
C7	D19-5		17
C9	D18-5		16
C11	D16-5		15
C13	E1-5		24
C15	D25-5		23
D2	D24-5		22
D4	D23-5		21
D6	D22-5		20
D8	E6-5		29
D10	E5-5		28
D12	E4-5		27
D14	E3-5		26
E1	E2-5		25
E3	E11-5		34
E5	E10-5		33
E11	E9-5		32
E13	E8-5		31
E15	E7-5		30
F2	E16-5		39
F4	E15-5		38
F12	E14-5		37

Unit Buffer Store	Designed K.H.A.	S 4	Drawing No	
	Approved		Drawn by <u>K.N.L.16.5.6</u>	
	Checked 1.2.63		Checked <u>F.E.23.10.67</u>	
	Last Revision		<div>2 Sheets</div> <div>Sheet 1</div>	


Pin	Wired To	Wired To	Name of Signal
F14	E13-5		36
G1	E12-5		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	F19-5		41
G15	E18-5		40
H2	Chassis		0 Volts
H4	H2-7		Busy
H6	G2-2		D
H8	F6-1		C
H10	G2-7		A
H12	S2-H12	S6-H12	Addr. 19
H14	S2-H14	S6-H14	Addr. 18
S1	S2-S1	S6-S1	Addr. 17
S3	S2-S3	S6-S3	Addr. 16
S5	S2-S5	S6-S5	Addr. 15
S7	S2-S7	S6-S7	Addr. 14
S9	S2-S9	S6-S9	Addr. 13
S11	S2-S11	S6-S11	Addr. 12
S13	S2-S13	S6-S13	Addr. 11
S15	S2-S15	S6-S15	Addr. 10
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: 6-3		

Unit Buffer Store	Designed K.H.A.	S 4	Drawing No	
	Approved		Drawn by L.N.L. 16.5.67	
	Checked 1.2.63		Checked F.F. 23.10.67	
	Last Revision		2 Sheets	Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	S3-A3		4
A5	S3-A5		3
A7	S3-A7		2
A9	S3-A9		1
A11	S3-A11		0
A13	S3-A13		0
A15	S3-A15		8
B2	S3-B2		7
B4	S3-B4		6
B6	S3-B6		5
B8	S3-B8		14
B10	S3-B10		13
B12	S3-B12		12
B14	S3-B14		11
C1	S3-C1		10
C3	S3-C3		19
C5	S3-C5		18
C7	S3-C7		17
C9	S3-C9		16
C11	S3-C11		15
C13	S3-C13		24
C15	S3-C15		23
D2	S3-D2		22
D4	S3-D4		21
D6	S3-D6		20
D8	S3-D8		29
D10	S3-D10		28
D12	S3-D12		27
D14	S3-D14		26
E1	S3-E1		25
E3	S3-E3		34
E5	S3-E5		33
E11	S3-E11		32
E13	S3-E13		31
E15	S3-E15		30
F2	S3-F2		39
F4	S3-F4		38
F12	S3-F12		37

Unit Buffer Store	Designed K.H.A	S 5	Drawing No	
	Approved		Drawn by L.N.L. 16.5.67	
	Checked 1.2.63		Checked F.E. 23-10-67	
	Last Revision		2 Sheets	Sheet 1


Pin	Wired To	Wired To	Name of Signal
F14	S3-F14		36
G1	S3-G1		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	S3-G13		41
G15	S3-G15		40
H2	S3-H2	S9-H2	Addr. 00
H4	H4-4		AWR3
H6	H7-9		
H8	H7-10		
H10	H7-13		
H12	S3-H12	S9-H12	Addr. 9
H14	S3-H14	S9-H14	Addr. 8
S1	Chassis		0 Volts
S3	Chassis		0 Volts
S5	S1-S5	S3-S5	AD1-5
S7	S3-S7		AD 4
S9	S3-S9		AD 3
S11	S3-S11		AD 2
S13	Chassis		0 Volts
S15	H5-11		
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: 6-2		

Unit Buffer/DFA200	Designed V.H.	S 5	Drawing No	
	Approved		Drawn by H.L. 26.3.68	
	Checked 6.3.68		Checked A. 27.3.68	
	Last Revision		2 Sheets	Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	D5-7		4
A5	D4-7		3
A7	D3-7		2
A9	D2-7		1
A11	D1-7		0
A13	D12-7		9
A15	D9-7		8
B2	D8-7		7
B4	D7-7		6
B6	D6-7		5
B8	D15-7		14
B10	D14-7		13
B12	D13-7		12
B14	D12-7		11
C1	D11-7		10
C3	D21-7		19
C5	D20-7		18
C7	D19-7		17
C9	D18-7		16
C11	D16-7		15
C13	E1-7		24
C15	D25-7		23
D2	D24-7		22
D4	D23-7		21
D6	D22-7		20
D8	E6-7		29
D10	E5-7		28
D12	E4-7		27
D14	E3-7		26
E1	E2-7		25
E3	E11-7		34
E5	E10-7		33
E11	E9-7		32
E13	E8-7		31
E15	E7-7		30
F2	E16-7		39
F4	E15-7		38
F12	E14-7		37 37

Unit Buffer Store	Designed K.H.A.	S 6	Drawing No
	Approved		Drawn by L.N.I. 16.5.67
	Checked 1.2.63		Checked F.E. 23-10-62
	Last Revision		2 Sheets Sheet 1

Pin	Wired To	Wired To	Name of Signal
F14	E13-7		36
G1	E12-7		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	F19-7		41
G15	E18-7		40
H2	Chassis		0 Volts
H4	H2-10		Busy
H6	G2-3		D
H8	F5-1		C
H10	G2-8		A
H12	S4-H12	S10-H12	Addr. 19
H14	S4-H14	S10-H14	Addr. 18
S1	S4-S1	S10-S1	Addr. 17
S3	S4-S3	S10-S3	Addr. 16
S5	S4-S5	S10-S5	Addr. 15
S7	S4-S7	S10-S7	Addr. 14
S9	S4-S9	S10-S9	Addr. 13
S11	S4-S11	S10-S11	Addr. 12
S13	S4-S13	S10-S13	Addr. 11
S15	S4-S15	S10-S15	Addr. 10
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: 6-3		

Unit Buffer Store	Designed K.H.A.	S 6	Drawing No
	Approved		Drawn by L.M.L. 16.5.67
	Checked 1.2.63		Checked F.E. 23.10.67
	Last Revision		2 Sheets

Pin	Wired To	Wired To	Name of Signal
A3	D5-26	S9-A3	4
A5	D4-26	S9-A5	3
A7	D3-26	S9-A7	2
A9	D2-26	S9-A9	1
A11	D1-26	S9-A11	0
A13	D10-26	S9-A13	9
A15	D9-26	S9-A15	8
B2	D8-26	S9-B2	7
B4	D7-26	S9-B4	6
B6	D6-26	S9-B6	5
B8	D15-26	S9-B8	14
B10	D14-26	S9-B10	13
B12	D13-26	S9-B12	12
B14	D12-26	S9-B14	11
C1	D11-26	S9-C1	10
C3	D21-26	S9-C3	19
C5	D20-26	S9-C5	18
C7	D19-26	S9-C7	17
C9	D18-26	S9-C9	16
C11	D16-26	S9-C11	15
C13	E1-26	S9-C13	24
C15	D25-26	S9-C15	23
D2	D24-26	S9-D2	22
D4	D23-26	S9-D4	21
D6	D22-26	S9-D6	20
D8	E6-26	S9-D8	29
D10	E5-26	S9-D10	28
D12	E4-26	S9-D12	27
D14	E3-26	S9-D14	26
E1	E2-26	S9-E1	25
E3	E11-26	S9-E3	34
E5	E10-26	S9-E5	33
E11	E9-26	S9-E11	32
E13	E8-26	S9-E13	31
E15	E7-26	S9-E15	30
F2	E16-26	S9-F2	39
F4	E15-26	S9-F4	38
F12	E14-26	S9-F12	37

Unit Buffer Store	Designed K.H.A.	S 7	Drawing No	
	Approved		Drawn by L.H.L. 16.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		2 Sheets Sheet 1	

Pin	Wired To	Wired To	Name of Signal
F14	E13-26	S9-F14	36
G1	E12-26	S9-G1	35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	E19-26	S9-G13	41
G15	E18-26	S9-G15	40
H2	E22-30		Addr. 00 <i>ref.</i>
H4	H3-28		AWP
H6	Chassis		0 Volts
H8	Chassis		0 Volts
H10	Chassis		0 Volts
H12	Chassis		0 Volts
H14	Chassis		0 Volts
S1	Chassis		0 Volts
S3	Chassis		0 Volts
S5	S3-S5	S9-S5	AD 1,5
S7	S3-S7	S9-S7	AD 1,4
S9	S3-S9	S9-S9	AD 1,3
S11	S3-S11	S9-S11	AD 1,2
S13	S11 - T14		<u>Control Select</u>
S15	B24-14		<u>Ext. Reset</u>
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: E-4		

Unit Buffer Store Designed K.H.A.

REGNE
CENTRALEN

Approved

Checked 1.2.63

Last Revision

S 7

Drawing No


Drawn by H.L. 16.5.67

Checked F.F. 23.10.67


2 Sheets

Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	D5-1		4
A5	D4-1		3
A7	D3-1		2
A9	D2-1		1
A11	D1-1		0
A13	D10-1		9
A15	D9-1		8
B2	D8-1		7
B4	D7-1		6
B6	D6-1		5
B8	D15-1		14
B11	D14-1		13
B12	D13-1		12
B14	D12-1		11
C1	D11-1		10
C3	D21-1		19
C5	D20-1		18
C7	D19-1		17
C9	D18-1		16
C11	D16-1		15
C13	E1-1		24
C15	D25-1		23
D2	D24-1		22
D4	D23-1		21
D6	D22-1		20
D8	E6-1		29
D10	E5-1		28
D12	E4-1		27
D14	E3-1		26
E1	E2-1		25
E3	E11-1		34
E5	E10-1		33
E11	E9-1		32
E13	E8-1		31
E15	E7-1		30
F2	E16-1		39
F4	E15-1		38
F12	E14-1		37

	Unit Buffer Store	Designed K.H.A.	S 8	Drawing No	
		Approved		Drawn by L.H.L. 16.5.67	
		Checked 1.2.63		Checked F.F. 23.10.67	
		Last Revision		2 Sheets	Sheet 1


Pin	Wired To	Wired To	Name of Signal
F14	E13-1		36
G1	E12-1		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	E19-1		41
G15	E18-1		40
H2	H2-27		Σ 7s.
H4	G1-2		Busy
H6	E22-4		<u>D</u> 0 BF \rightarrow Gen
H8	F8-1		<u>C</u> 0 T \emptyset
H10	E22-6		<u>H</u> 0 AC
H12	H1-6		<u>AD</u> 1,9
H14	H1-4		<u>AD</u> 1,8
S1	H1-1		<u>AD</u> 1,7
S3	Chassis		0 Volts
S5	Chassis		0 Volts
S7	H1-7		AD 1,9
S9	H1-5		AD 1,8
S11	H1-3		AD 1,7
S13	Chassis		0 Volts
S15	H6-32		<u>AD</u> 1-6
T2	H8-35		AD1-6
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
Code: 6-5			

UniBuffer/DFA200	Designed V.H.	S 8	Drawing No
	Approved		Drawn by N. L. 26.3.68
	Checked 6.3.68		Checked I.K. 27.3.68
	Last Revision		2 Sheets Sheet 2


Pin	Wired To	Wired To	Name of Signal
A3	S7-A3		4
A5	S7-A5		3
A7	S7-A7		2
A9	S7-A9		1
A11	S7-A11		0
A13	S7-A13		9
A15	S7-A15		8
B2	S7-B2		7
B4	S7-B4		6
B6	S7-B6		5
B8	S7-B8		14
B10	S7-B10		13
B12	S7-B12		12
B14	S7-B14		11
C1	S7-C1		10
C3	S7-C3		19
C5	S7-C5		18
C7	S7-C7		17
C9	S7-C9		16
C11	S7-C11		15
C13	S7-C13		24
C15	S7-C15		23
D2	S7-D2		22
D4	S7-D4		21
D6	S7-D6		20
D8	S7-D8		29
D10	S7-D10		28
D12	S7-D12		27
D14	S7-D14		26
E1	S7-E1		25
E3	S7-E3		34
E5	S7-E5		33
E11	S7-E11		32
E13	S7-E13		31
E15	S7-E15		30
F2	S7-E2		39
F4	S7-F4		38
F12	S7-F12		37

Unit Buffer Store		Designed K.H.A.	S 9		Drawing No	
		Approved			Drawn by L.N.L. 16.5.67	
		Checked 1.2.63			Checked F.E. 23-10-62	
		Last Revision			2 Sheets Sheet 1	


Pin	Wired To	Wired To	Name of Signal
F14	S7-F14		36
G1	S7-G1		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	S7-G13		41
G15	S7-G15		40
H2	S5-H2		Addr. 00
H4	H4- 6		AWR 4
H6	H8-22		
H8	H8-24		
H10	H8-26		
H12	S5-H12		Addr. 9
H14	S5-H14		Addr. 8
S1	 		
S3	Chassis		0 Volts
S5	S7-S5		AD 5
S7	S7-S7		AD 4
S9	S7-S9		AD 3
S11	S7-S11		AD 2
S13	Chassis		0 Volts
S15	H5-10		
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: 6-2		

Unit Buffer Store	Designed K.H.A.	S 9	Drawing No
	Approved		Drawn by L.N.L. 16.5.67
	Checked 1.2.63		Checked F.E. 23.10.67
	Last Revision		2 Sheets Sheet 2

Pin	Wired To	Wired To	Name of Signal
A3	D5-9		4
A5	D4-9		3
A7	D3-9		2
A9	D2-9		1
A11	D1-9		0
A13	D10-9		9
A15	D9-9		8
B2	D8-9		7
B4	D7-9		6
B6	D6-9		5
B8	D15-9		14
B10	D14-9		13
B12	D13-9		12
B14	D12-9		11
C1	D11-9		10
C3	D21-9		19
C5	D20-9		18
C7	D19-9		17
C9	D18-9		16
C11	D16-9		15
C13	E1-9		24
C15	D25-9		23
D2	D24-9		22
D4	D23-9		21
D6	D22-9		20
D8	E6-9		29
D10	E5-9		28
D12	F4-9		27
D14	E3-9		26
E1	E2-9		25
E3	F11-9		34
E5	E10-9		33
E11	F9-9		32
E13	E8-9		31
E15	F7-9		30
F2	E16-9		39
F4	F15-9		38
F12	F14-9		37

Unit Buffer Store	Designed K.H.A.	S 10	Drawing No
 CENTRALEN	Approved		Drawn by L.N.L.16.5.67
	Checked 1.2.63		Checked F.E. 23/0.42
	Last Revision		2 Sheets Sheet 1

Pin	Wired To	Wired To	Name of Signal
F14	E13-9		36
G1	E12-9		35
G3	Chassis		0 Volts
G5	Chassis		0 Volts
G11	Chassis		0 Volts
G13	F10-9		41
G15	E18-9		40
H2	Chassis		0 Volts
H4	H2-22		Busy
H6	G2-4		D
H8	F4-1		C
H10	G2-9		A
H12	S6-H12		Addr. 19
H14	S6-H14		Addr. 18
S1	S6-S1		Addr. 17
S3	S6-S3		Addr. 16
S5	S6-S5		Addr. 15
S7	S6-S7		Addr. 14
S9	S6-S9		Addr. 13
S11	S6-S11		Addr. 12
S13	S6-S13		Addr. 11
S15	S6-S15		Addr. 10
T2			
T4			
T6			
T8			
T10			
T12			
T14			
U1			
U3			
U5			
U7			
U9			
U11			
U13			
U15			
	Code: 6-3		

Unit Buffer Store 	Designed K.H.A.	S 10	Drawing No	
	Approved		Drawn by L.N.L. 16.5.67	
	Checked 1.2.63		Checked F.E. 23.10.67	
	Last Revision		2 Sheets	Sheet 2

Pin	Wired To	Wired To	Name of Signal
A	D1-27	S3-A11	^ LINE 0
B	D2-27	S3-A9	- 1
C	D3-27	S3-A7	- 2
D	D4-27	S3-A5	- 3
E	D5-27	S3-A3	- 4
F	D6-27	S3-B6	- 5
H	D7-27	S3-B4	- 6
J	D8-27	S3-B2	- 7
K	D9-27	S3-A15	- 8
L	D10-27	S3-A13	- 9
M	D11-27	S3-C1	- 10
N	D12-27	S3-B14	- 11
P	D13-27	S3-C12	- 12
R	D14-27	S3-B10	- 13
S	D15-27	S3-B8	- 14
T	D16-27	S3-C11	- 15
U	D18-27	S3-C9	- 16
V	D19-27	S3-C7	- 17
W	D20-27	S3-C5	- 18
X	D21-27	S3-C3	- 19
Y	D22-27	S3-D6	- 20
Z	D23-27	S3-D4	- 21
AA	D24-27	S3-D2	- 22
BB	D25-27	S3-C15	- 23
CC	E1-27	S3-C13	- 24
DD	E2-27	S3-E1	- 25
EE	E3-27	S3-D14	- 26
FF	E4-27	S3-D12	- 27
HH	E5-27	S3-D10	- 28
JJ	E6-27	S3-D8	- 29
KK	E7-27	S3-E15	- 30
LL	E8-27	S3-F13	- 31
MM	E9-27	S3-E11	- 32
NN	E10-27	S3-E5	- 33
PP	D23-15		0 Volts
RR	D22-15		0 Volts
SS	D21-15		0 Volts
TT	D20-15		0 Volts

Unit: Buffer/DFA20

Designed V.H.



Approved 6.3.68

Checked

Last Revision

J 8
Data Lines to Disk
Code: S2-2

Drawing No

Drawn by N.1.14.3.8

Checked J.K. 15.3.1968

1 Sheets

Sheet 1

Pin	Wired To	Wired To	Name of Signal
A	E11-27	S3-E3	^ LINE 34
B	E12-27	S3-G1	- 35
C	E13-27	S3-F14	- 36
D	E14-27	S3-F12	- 37
E	E15-27	S3-F4	- 38
F	E16-27	S3-F2	- 39
H	E18-27	S3-G15	- 40
J	E19-27	S3-G13	- 41
K	E19-15		0 Volts
L	E20-15		0 Volts
M	E22-7	S3-H2	^ ADR 00
N	D1-1		- 0
P	D2-1		- 1
R	D3-1		- 2
S	D4-1		- 3
T	D5-1		- 4
U	D6-1		- 5
V	D7-1		- 6
W	D8-1		- 7
X	D9-1	S3-H14	- 8
Y	D10-1	S3-H12	- 9
Z	D11-1	S4-S15	- 10
AA	D12-1	S4-S13	- 11
BB	D13-1	S4-S11	- 12
CC	D14-1	S4-S9	- 13
DD	D15-1	S4-S7	- 14
EE	D16-1	S4-S5	- 15
FF	D18-1	S4-S3	- 16
HH	D19-1	S4-S1	- 17
JJ	D20-1	S4-H14	- 18
KK	D21-1	S4-H12	- 19
LL	D22-1		- 20
MM	D23-1		- 21
NN			- 22
PP	D19-15		0 Volts
RR	D18-15		0 Volts
SS	D16-15		0 Volts
TT	D15-15		0 Volts

Unit Buffer/DFA200

Designed V.H.

REGNE

CENTRALEN

Approved

Checked 6.3.68

Last Revision

J9

Data Lines to Disk
Code: S2-3

Drawing No

Drawn by L.N.L.14.3.6

Checked 14.15.2.1968

1 Sheets

Sheet 1

Pin	Wired To	Wired To	Name of Signal
A	D1-3		^ LINE 0
B	D2-3		- 1
C	D3-3		- 2
D	D4-3		- 3
E	D5-3		- 4
F	D6-3		- 5
H	D7-3		- 6
J	D8-3		- 7
K	D9-3		- 8
L	D10-3		- 9
M	D11-3		- 10
N	D12-3		- 11
P	D13-3		- 12
R	D14-3		- 13
S	D15-3		- 14
T	D16-3		- 15
U	D18-3		- 16
V	D19-3		- 17
W	D20-3		- 18
X	D21-3		- 19
Y	D22-3		- 20
Z	D23-3		- 21
AA	D24-3		- 22
BB	D25-3		- 23
CC	E1-3		- 24
DD	E2-3		- 25
EE	E3-3		- 26
FF	E4-3		- 27
HH	E5-3		- 28
JJ	E6-3		- 29
KK	E7-3		- 30
LL	E8-3		- 31
MM	E9-3		- 32
NN	E10-3		- 33
PP	D14-15		0 Volts
RR	D13-15		0 Volts
SS	D12-15		0 Volts
TT	D11-15		0 Volts

Unit Buffer/DFA200

Designed V.H.

REGNE
CENTRALEN

Approved

Checked 6.3.68

Last Revision

J10

Data Lines from Disk

Code: S2-4

Drawing No

Drawn by N.L.14.3.68

Checked I.K. 15.3.1968

1 Sheets

Sheet 1

Pin	Wired To	Wired To	Name of Signal
A	E11-3		^ LINE 34
B	E12-3		- 35
C	E13-3		- 36
D	E14-3		- 37
E	E15-3		- 38
F	E16-3		- 39
H	E18-3		- 40
J	E19-3		- 41
K	E22-15		0 Volts
L	E21-15		0 Volts
M	E18-15		0 Volts
N	E16-15		0 Volts
P	B24-14		^ Reset
R	E15-15		0 Volts
S	G2-1		^ D
T	F7-1		^ C
U	G2-6		^ A
V	E14-15		0 Volts
W	H5-13		INTERLOCK
X	E13-15		0 Volts
Y	E12-15		0 Volts
Z	E11-15		0 Volts
AA	E10-15		0 Volts
BB	H4-2		^ AWR
CC	H2-3		^ BUSY
DD	H2-15		0 Volts
EE	H3-15		0 Volts
FF	H4-15		0 Volts
HH	H5-15		0 Volts
JJ	S5-S5		^ AD1-5
KK	H6-4		^ AD1-6
LL	H6-3		^ AD1-7
MM	H6-2		^ AD1-8
NN	H6-1		^ AD1-9
PP	H2-21		0 Volts
RR	H3-21		0 Volts
SS	H4-21		0 Volts
TT	H5-21		0 Volts

Unit Buffer/DFA200

Designed V.H



Approved

Checked 6.3.68

Last Revision

J11

Data Lines from Disk

Code: S2-5


Drawing No

Drawn by N.L. 14.3.68

Checked I.A. 15.3.1968

1 Sheets

Sheet 1

	Unit Buffer Store	Designed K.H.A.	Wiring Schedule	Drawing No
	Approved	Checked 1.2.63.		Drawn by L.L.23.2.66.
	Last Revision			Checked F.E.23-10-67
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PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15						15
16						16
17						17
18						18
19						19
20						20
21						21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35

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PIN	Special Wire	Wired To	Wired To	—x—	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15						15
16						16
17						17
18						18
19						19
20						20
21						21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35

Unit Buffer Store REGNE CENTRALEN	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved		Drawn by L.L.23.2.66	
	Checked 1.2.03.		Checked F.E.23.10.67	
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REGNE CENTRALEN	Unit: Buffer Store	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved Checked 1.2.63. Last Revision			Drawn by J.L. 23.2.66	
				Checked F.E. 23.10.67	
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				A 19	1232-1

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1	+ 24 Volts	A19-2		- x	+ 24 Volts	1
2	+ 24 Volts	A19-1		- x	+ 24 Volts	2
3	+ 24 Volts	A19-4		- x	+ 24 Volts	3
4	+ 24 Volts	A19-3		- x	+ 24 Volts	4
5	+ 24 Volts	A19-6		- x	+ 24 Volts	5
6	+ 24 Volts	A19-5		- x	+ 24 Volts	6
7					Iry	7
8			C8-12		Iry	8
9			C8-13		Iry	9
10	0 Volts			- x	0 Volts	10
11	0 Volts	A19-12		- x	0 Volts	11
12	0 Volts	A19-11		- x	0 Volts	12
13	- 1.6 Volts	C18-10		- x	- 1.6 Volts	13
14	- 1.6 Volts	A19-15		- x	- 1.6 Volts	14
15	- 1.6 Volts	A19-14		- x	- 1.6 Volts	15
16			C18-10			16
17						17
18						18
19						19
20						20
21						21
22						22
23		A21-23		- x	Iry	23
24	0 Volts	A19-25		- x	0 Volts	24
25	0 Volts	A19-24		- x	0 Volts	25
26	- 3.2 Volts	A19-27		- x	- 3.2 Volts	26
27	- 3.2 Volts	A19-26		- x	- 3.2 Volts	27
28			C18-31			28
29		C8-10			Iry	29
30		C8-11			Iry	30
31					Iry	31
32		B21-35			Ry	32
33	- 24 Volts	A19-34		- x	- 24 Volts	33
34	- 24 Volts	A19-33		- x	- 24 Volts	34
35	- 24 Volts			- x	- 24 Volts	35

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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1			C22-29	- x -		1
2				- x -		2
3				- x -		3
4				- x -		4
5				- x -		5
6				- x -		6
7						7
8						8
9						9
10				- x -		10
11				- x -		11
12				- x -		12
13				- x -		13
14				- x -		14
15	- 1.6 Volts		- 1.6 V Term. P.S.	- x -	- 1.6 Volts	15
16						16
17						17
18						18
19						19
20						20
21						21
22						22
23						23
24	0 Volts		A22-21	- x -	0 Volts	24
25				- x -		25
26				- x -		26
27				- x -		27
28						28
29						29
30						30
31						31
32						32
33				- x -		33
34			B22-32	- x -		34
35	- 24 Volts		- 24 V Term. P.S.	- x -	- 24 Volts	35

Unit: BufferStore

Designed K.H.A.

Approved

Checked 1.2.63.

Last Revision

Wiring Schedule

Drawing No

Drawn by L.L.23.2.66.

Checked F.E.23.4.62

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REGNE
CENTRALEN

PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1	+ 24 Volts	+ 24 V Term.P.S.		x -	+ 24 Volts	1
2	+ 24 Volts	A21-3		x -	+ 24 Volts	2
3	+ 24 Volts	A21-2		x -	+ 24 Volts	3
4	+ 24 Volts	A21-5		x -	+ 24 Volts	4
5	+ 24 Volts	A21-4		x -	+ 24 Volts	5
6	+ 24 Volts	+ 24 V Term.P.S.		x -	+ 24 Volts	6
7					Irx	7
8		C16-12			Irx	8
9		C16-13			Irx	9
10	0 Volts	A21-11		x -	0 Volts	10
11	0 Volts	A21-10	A22-15	x -	0 Volts	11
12	0 Volts	A22-15		x -	0 Volts	12
13	- 1.6 Volts	A21-14		x -	- 1.6 Volts	13
14	- 1.6 Volts	A21-13		x -	- 1.6 Volts	14
15	- 1.6 Volts			x -	- 1.6 Volts	15
16						16
17						17
18						18
19						19
20						20
21						21
22						22
23		B21-27	A19-23	x -	4x	23
24	0 Volts			x -	0 Volts	24
25	0 Volts			x -	0 Volts	25
26	- 3.2 Volts	A21-27		x -	- 3.2 Volts	26
27	- 3.2 Volts	- 3.2 V Term.P.S.	A21-26	x -	- 3.2 Volts	27
28					Iwx	28
29		C16-10			Iwx	29
30		C16-11			Iwx	30
31					Rx	31
32		B22-28			Rx	32
33	- 24 Volts			x -	- 24 Volts	33
34	- 24 Volts	A21-35		x -	- 24 Volts	34
35	- 24 Volts	A21-34		x -	- 24 Volts	35

Unit: Buffer Store



CENTRALEN

Designed K.M.A.

Approved

Checked 1.2.63.

Last Revision

Wiring Schedule

Drawing No

Drawn by L.L.23.2.66.

Checked F.E.23.10.67

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REGNE CENTRALEN	Unit: Buffer Store	Designed K.M.N.	Drawing No Drawn by L.L.L. 23.2.66. Checked F.F. 23.10.67 10 Sheets Sheet 1 A 22
		Approved	
	Checked 1.2.63.	Wiring Schedule	
	Last Revision		

PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15			A21-12	- x		15
16						16
17						17
18						18
19						19
20						20
21			A20-24	- x		21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35

REGNE CENTRALEN	Unit Buffer Store	Designed K.H.A.	Drawing No Drawn by L.L.23.2.66. Checked F.E.23-10-67 10 Sheets Sheet 8 A 23
	Approved		
	Checked 1.2.63.		
	Last Revision		
	Wiring Schedule		

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signer
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15				- x -	
16					
17					
18					
19					
20					
21				- x -	
22					
23					
24					
25					
26					
27					
28					
29					
30					
31					
32					
33					
34					
35					

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Unit: Buffer Store  REGNE CENTRALEN	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved		Drawn by L.L.23.2.66.	
	Checked 1.2.63.		Checked F.E.29.10.67	
	Last Revision		10 Sheets Sheet 2 A24	

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15				- x -		15
16						16
17						17
18						18
19						19
20						20
21				- x -		21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15				x		15
16						16
17						17
18						18
19						19
20						20
21				x		21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35

Unit Buffer Store REGNE CENTRALEN	Designed A. H. .	Wiring Schedule	Drawing No	
	Approved		Drawn by L. L. 3-66	
	Checked 1.2.63.		Checked F. F. 23-10-67	
	Last Revision		10 Sheets	Sheet 10
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REGNE CENTRALEN	Unit Buffer Store	Designed KPHZAT	Wiring Schedule	Drawing No
	Approved	Drawn by L.L.27.2.66.		Checked F.E.23.10.67
	Checked 1.2.68.	10 Sheets		Sheet 2
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PIN	Special Wire	Wired To	Wired To	— x —	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6						6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14						14
15						15
16						16
17						17
18						18
19						19
20						20
21						21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32						32
33						33
34						34
35						35


pos. B1 - B17

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1		B18-35				1
2		B18-10			IGP TR --> BR	2
3		E9-23			Strobe TR 33-42	3
4		E20-23			Strobe TR 24-32	4
5		D12-23			Strobe TR 0-11	5
6		D13-23			Strobe TR 12-23	6
7		B18-15				7
8	+ 8 Volts	C18-28			+ 8 Volts	8
9	- 8 Volts	B19-13			- 8 Volts	9
10		B18-2	C18-9			10
11		B18-12	B18-11			11
12		B18-13	B18-10			12
13		B18-12	B18-11			13
14		F12-29			AD 00 In	14
15	0 Volts	B18-7		- x	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts	B18-27		- x	0 Volts	21
22		B18-30				22
23		E9-22			IGP TR 33-42	23
24		E20-22			IGP TR 24-32	24
25		D12-22			IGP TR 0-11	25
26		D13-22			IGP TR 12-23	26
27		B18-21				27
28	+ 8 Volts	B19-22			+ 8 Volts	28
29	- 8 Volts				- 8 Volts	29
30		B18-22	B18-31			30
31		B18-32	B18-30			31
32		B18-33	B18-31			32
33		B18-32				33
34		F12-24			AD 00 In	34
35		B18-1	B19-32		Strobe Prim.	35


Unit: Buffer store  CENTRALEN	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved		Drawn by J. E. 23.10.67	
	Checked 1-2-63-		Checked F.E. 23.10.67	
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Unit: Buffer Store 	Designed K.M.A.	Wiring Schedule	Drawing No	
	Approved		Drawn by L.L. 15.3.66.	
	Checked 1.2.63.		Checked F.F. 29.10.67	
	Last Revision		10 Sheets Sheet 4 B 19	

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1						1
2						2
3						3
4						4
5						5
6			B21-34		Rty	6
7						7
8						8
9						9
10			B19-33			10
11	0 Volts		B21-15		0 Volts	11
12						12
13	- 8 Volts		B18-9	- x	- 8 Volts	13
14						14
15	0 Volts			- x	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts		B19-25	- x	0 Volts	21
22	+ 8 Volts		B18-28	- x	+ 8 Volts	22
23						23
24						24
25	0 Volts		B19-21		0 Volts	25
26						26
27						27
28						28
29						29
30						30
31						31
32			B18-35		Strobe Prim.	32
33			B19-10			33
34						34
35						35

Unit: Buffer Store 	Designed K.H.A.	Wiring Schedule	Drawing No 1	
	Approved		Drawn by L.H.L. 24.5.66	
	Checked 1.2.63.		Checked F.E. 29.10.67	
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			B 20	1007-2


PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1						1
2		B24-29	B21-35		Ir Ry In	2
3		B21-4				3
4						4
5						5
6						6
7						7
8		B21-29			wt In	8
9		B21-8				9
10						10
11						11
12	- 24 Volts	B21-32	C20-27		- 24 Volts	12
13	- 8 Volts	B21-25		x -	- 8 Volts	13
14						14
15	0 Volts			- x -	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x -	0 Volts	21
22	+ 8 Volts	B21-33		x -	+ 8 Volts	22
23						23
24						24
25						25
26						26
27						27
28						28
29						29
30						30
31						31
32		B23-29			End Write Out	32
33						33
34		B23-30			End Read Out	34
35						35

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1	0 Volts	B22-15		- x	0 Volts	1
2		B24-30	B22-28		Ir Rx In	2
3	0 Volts	B21-5		- x	0 Volts	3
4		B20-3		- x	End Read In	4
5	0 Volts	B21-3		- x	0 Volts	5
6		B22-27			Ir Ry In	6
7	0 Volts	B21-9		- x	0 Volts	7
8		B21-12	B20-9		End Write	8
9	0 Volts	B21-7		- x	0 Volts	9
10		B21-31			En In	10
11	0 Volts			- x	0 Volts	11
12		B21-8	B23-8		End Read In	12
13	+ 8 Volts	B20-22		- x	+ 8 Volts	13
14	0 Volts			- x	0 Volts	14
15	0 Volts	B19-11		- x	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x	0 Volts	21
22		B21-23		- x	Aut. Reset In	22
23		B21-22		- x	Aut. Reset In	23
24				- x	Aut. Reset In	24
25	- 8 Volts	B20-13		- x	- 8 Volts	25
26						26
27		A21-23			Wt	27
28		B24-35	B20-8			28
29						29
30		B23-34			Inhibit Pulse	30
31		B21-10	B24-25		Inhibit Pulse	31
32	- 24 Volts	B20-12		- x	- 24 Volts	32
33						33
34		B19-5			Ir Ry Out	34
35		B20-2	A19-32		Ir Ry Out	35

REGNE CENTRALEN	Unit: Buffer Store	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved Checked 1.2.6J. Last Revision	Wiring Schedule		Drawn by L.L.14.3.66.	
				Checked F.E.29.10.67	
				10 Sheets	Sheet I
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1	0 Volts	B22-3		x -	0 Volts	1
2		F3-7				2
3	0 Volts	B22-1		x -	0 Volts	3
4		B22-8		x -	End Read In	4
5	0 Volts	B22-7		x -	0 Volts	5
6		B22-35				6
7	0 Volts	B22-5		x -	0 Volts	7
8		B22-12	B22-4		End Read In	8
9	0 Volts	B22-11		x -	0 Volts	9
10		B22-31			Rt	10
11	0 Volts	B22-9		x -	0 Volts	11
12		B22-8	B23-7		End Read In	12
13	+ 8 Volts	B24-31		x -	+ 8 Volts	13
14	0 Volts			x -	0 Volts	14
15	0 Volts	B21-1		- x -	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x -	0 Volts	21
22		B24-32		x -	Aut. Reset-In	22
23		B22-24		x -	Aut. Reset In	23
24		B22-23		x -	Aut. Reset In	24
25	- 8 Volts	B23-5		x -	- 8 Volts	25
26						26
27		B21-6				27
28		B21-2	A21-32		Ir Rx	28
29						29
30		B23-35			Rt Out	30
31		B22-10	B24-33		Rt Out	31
32	- 24 Volts	A20-34		x -	- 24 volts	32
33						33
34						34
35		B22-6	B24-34			35

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Unit: Buffer Store 	Designed K. H. A.	Wiring Schedule	Drawing No	
	Approved		Drawn by <i>Lehald, J. 666</i>	
	Checked 1.2.63.		Checked <i>F. E. 23-10-67</i>	
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1		C25-13			Rt A and B Out	1
2		B23-31				2
3		C25-14				3
4		D22-29			Inhibit Pulse 1-23	4
5	- 8 Volts	B24-23	B22-25		- 8 Volts	5
6		E20-29			Inhibit Pulse 24-42	6
7		B22-12			End Read	7
8		B21-12			End Write	8
9						9
10						10
11						11
12						12
13						13
14						14
15	C Volts			- x -	C Volts	15
16						16
17						17
18						18
19						19
20						20
21	C Volts			- x -	C Volts	21
22						22
23						23
24						24
25						25
26						26
27						27
28						28
29		B20-32			End Write	29
30		B20-34			End Read In	30
31		B23-2	B23-32			31
32		B23-31	B23-33			32
33		B23-32				33
34		B21-30			Inhibit Pulse	34
35		B22-30			Rt	35

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PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1						1
2						2
3						3
4	- 1.6 Volts	C24-10			- 1.6 Volts	4
5						5
6		F7-12			Clock Out	6
7						7
8						8
9						9
10						10
11						11
12						12
13						13
14		S7-S15	J11-P		Reset	14
15	0 Volts	Chassis		-x-	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			-x-	0 Volts	21
22		F8-22			Reset	22
23	- 8 Volts	B23-5	G1-3		- 8 Volts	23
24			- 8 V Term. P.S.			24
25		B21-31			Inhibit Pulse	25
26						26
27						27
28						28
29		B20-2			Ir Rx In	29
30		B21-2			Ir Rx In	30
31	+ 8 Volts	B22-13	+ 8 V Term. P.S.		+ 8 Volts	31
32		B22-22			Aut. Reset	32
33		B22-31			Rt In	33
34		B22-35			Start In	34
35		B21-28			Wt In	35

Unit Buffer Store REGNE CENTRALEN	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved		Drawn by L. L. 23.2.66	
	Checked 1.2.63.		Checked F. L. 23.10.67	
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			B 25	

PIN	Special Wire	Wired To	Wired To	Name of Signal	PIN
1					1
2					2
3					3
4					4
5					5
6					6
7					7
8					8
9					9
10					10
11					11
12					12
13					13
14					14
15	0 Volts		x -	0 Volts	15
16					16
17					17
18					18
19					19
20					20
21	0 Volts		x -	0 Volts	21
22					22
23					23
24					24
25					25
26					26
27					27
28					28
29					29
30					30
31					31
32					32
33					33
34					34
35					35


Unit: Buffer Store	Designed K.H.A.	Crosswiring at Frame C	Drawing No. Drawn by I.K.T.5.6 Checked F.F.29.10.67 <div style="display: flex; justify-content: space-between;"> 26 Sheets Sheet 1 </div>
Approved Checked 1.2.63 Last Revision			

REGNE CENTRALEN	Unit Buffer Store	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved	Approved		Drawn by L.L.12.J.66.	
	Checked 1.2.63.	Checked		F.E.22.10.62	
	Last Revision	26 Sheets		Sheet 2	
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-0y	4
5				- x -	WA-7y	5
6				- x -	WA-3y	6
7				- x -	WA-5y	7
8				- x -	WA-1y	8
9			C22-35	- x -	WB-0y	9
10				- x -	Wy	10
11				- x -	Wy	11
12				- x -	Ry	12
13				- x -	Ry	13
14			C22-34	- x -	RB-0y	14
15				- x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5y	21
22				- x -	RA-3y	22
23				- x -	RA-7y	23
24				- x -	RA-0y	24
25				- x -	RA-4y	25
26				- x -	RA- -y	26
27				- x -	RA-6y	27
28		C5-C32			C5 Driving	28
29		C5-C31			C5 Driving	29
30		C5-C30			C5 Driving	30
31		C5-C29			C5 Driving	31
32		C5-C28			C5 Driving	32
33		C5-C27			C5 Driving	33
34		C5-C26			C5 Driving	34
35		C5-C25			C5 Driving	35

REGNE CENTRALEN	Unit Buffer Board	Designed A. T. A.	Wiring Schedule	Drawing No	
	Approved	Checked 1.2.62.		Drawn by L. L. 15.3.66	
	Last Revision			Checked F. E. 23.10.67	
				26 Sheets	Sheet 3
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PIN	Special Wire	Wired To	Wired To	— x —	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-7y	4
5				- x -	WA-3y	5
6				- x -	WA-5y	6
7				- x -	WA-4y	7
8				- x -	WA-4y	8
9				- x -	WA-4y	9
10			C22-33	- x -	WA-4y	10
11				- x -	WA-4y	11
12				- x -	WA-4y	12
13				- x -	WA-4y	13
14			C22-32	- x -	WA-4y	14
15				- x -	WA-4y	15
16				- x -	WA-4y	16
17				- x -	WA-4y	17
18				- x -	WA-4y	18
19				- x -	WA-4y	19
20				- x -	WA-4y	20
21				- x -	WA-4y	21
22				- x -	WA-4y	22
23				- x -	WA-4y	23
24				- x -	WA-4y	24
25				- x -	WA-4y	25
26				- x -	WA-4y	26
27				- x -	WA-4y	27
28			C5-C24	- x -	CS Driving	28
29			C5-C23	- x -	CS Driving	29
30			C5-C22	- x -	CS Driving	30
31			C5-C21	- x -	CS Driving	31
32			C5-C20	- x -	CS Driving	32
33			C5-C19	- x -	CS Driving	33
34			C5-C18	- x -	CS Driving	34
35			C5-C17	- x -	CS Driving	35

 REGNE CENTRALEN	Unit Buffer 1000	Designed 10.10.80	Wiring Schedule	Drawing No
	Approved	Checked 10.2.83		Drawn by L. L. 10.10.80
	Last Revision	Checked 10.2.83		26 Sheets
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-0y	4
5				- x -	WA-7y	5
6				- x -	WA-3y	6
7				- x -	WA-5y	7
8				- x -	WA-1y	8
9				- x -	WB-2y	9
10			C22-31	- x -	WY	10
11				- x -	WY	11
12				- x -	RY	12
13				- x -	RY	13
14			C22-30	- x -	RB-2y	14
15				- x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5y	21
22				- x -	RA-3y	22
23				- x -	RA-7y	23
24				- x -	RA-0y	24
25				- x -	RA-4y	25
26				- x -	RA-2y	26
27				- x -	RA-6y	27
28			CS-C16		CS Driving	28
29			CS-C15		CS Driving	29
30			CS-C14		CS Driving	30
31			CS-C13		CS Driving	31
32			CS-C12		CS Driving	32
33			CS-C11		CS Driving	33
34			CS-C10		CS Driving	34
35			CS-C9		CS Driving	35

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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-0y	4
5				- x -	WA-7y	5
6				- x -	WA-3y	6
7				- x -	WA-5y	7
8				- x -	WA-1y	8
9			C22-26		WB-6y	9
10				- x -	WY	10
11				- x -	WY	11
12				- x -	RY	12
13				- x -	RY	13
14			C22-23		RB-6y	14
15				- x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5y	21
22				- x -	RA-3y	22
23				- x -	RA-7y	23
24				- x -	RA-0y	24
25				- x -	RA-4y	25
26				- x -	RA-2y	26
27				- x -	RA-6y	27
28		CS-C8			CS Driving	28
29		CS-C7			CS Driving	29
30		CS-C6			CS Driving	30
31		CS-C5			CS Driving	31
32		CS-C4			CS Driving	32
33		CS-C3			CS Driving	33
34		CS-C2			CS Driving	34
35		CS-C1			CS Driving	35

REGNE CENTRALEN	Unit: Buffer Store	Designed: K.H.V.	Wiring Schedule	Drawing No	
		Approved		Drawn by L.L.15.3.66.	
		Checked: 1.2.63.		Checked F.E. 23.10.67	
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Unit: Buffer Store  REGNE CENTRALEN	Designed K.H.H.	Wiring Schedule	Drawing No	
	Approved		Drawn by L.L.15.3.66	
	Checked 1.2.63.		Checked F.E.23.10.62	
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-0y	4
5				- x -	WA-7y	5
6				- x -	WA-3y	6
7				- x -	WA-5y	7
8				- x -	WA-1y	8
9			C23-35	- x -	WB-1y	9
10				- x -	WY	10
11				- x -	WY	11
12				- x -	RY	12
13				- x -	RY	13
14			C23-34	- x -	RB-1y	14
15				- x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5y	21
22				- x -	RA-3y	22
23				- x -	RA-7y	23
24				- x -	RA-0y	24
25				- x -	RA-4y	25
26				- x -	RA-2y	26
27				- x -	RA-6y	27
28		CS-A32			CS Driving	28
29		CS-A31		- x -	CS Driving	29
30		CS-A30		- x -	CS Driving	30
31		CS-A29		- x -	CS Driving	31
32		CS-A28		- x -	CS Driving	32
33		CS-A27		- x -	CS Driving	33
34		CS-A26		- x -	CS Driving	34
35		CS-A25		- x -	CS Driving	35

PIN	Special Wire	Wired To	Wired To	Wired To	Name of Signal	PIN
1					WA-6y	1
2					WA-2y	2
3					WA-4y	3
4					WA-0y	4
5					WA-7y	5
6					WA-3y	6
7					WA-5y	7
8					WA-1y	8
9					WB-5y	9
10			C23-33		WY	10
11					WY	11
12					RY	12
13					RY	13
14			C23-32		RB-5y	14
15					RA-1y	15
16						16
17						17
18						18
19						19
20						20
21					RA-5y	21
22					RA-3y	22
23					RA-7y	23
24					RA-0y	24
25					RA-4y	25
26					RA-2y	26
27					RA-6y	27
28			C5-A24		C5 Driving	28
29			C5-A23		C5 Driving	29
30			C5-A22		C5 Driving	30
31			C5-A21		C5 Driving	31
32			C5-A20		C5 Driving	32
33			C5-A19		C5 Driving	33
34			C5-A18		C5 Driving	34
35			C5-A17		C5 Driving	35

REGNE CENTRALEN	Unit: Buffer Store	Designed K.H.A.	Wiring Schedule	Drawing No	
	Approved	Checked 1.2.63.		Drawn by L.L.15.3.66.	
	Last Revision			Checked F.E. 23-10-67	
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	Unit: Buffer store	Designed: N. 1. .	Wiring Schedule	Drawing No	
		Approved		Drawn by: l.n.1.15.3.66.	
		Checked: 1.2.63.		Checked: F.F.23-10-67	
		Last Revision		26 Sheets	Sheet 8
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PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6y	1
2				- x -	WA-2y	2
3				- x -	WA-4y	3
4				- x -	WA-0y	4
5				- x -	WA-7y	5
6				- x -	WA-3y	6
7				- x -	WA-5y	7
8				- x -	WA-1y	8
9				- x -	WB-3y	9
10			C23-31	- x -	WY	10
11				- x -	WY	11
12				- x -	RY	12
13				- x -	RY	13
14			C23-30	- x -	RB-3y	14
15				- x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5y	21
22				- x -	RA-3y	22
23				- x -	RA-7y	23
24				- x -	RA-0y	24
25				- x -	RA-4y	25
26				- x -	RA-2y	26
27				- x -	RA-6y	27
28			CS-A16		CS Driving	28
29			CS-A15		CS Driving	29
30			CS-A14		CS Driving	30
31			CS-A13		CS Driving	31
32			CS-A12		CS Driving	32
33			CS-A11		CS Driving	33
34			CS-A10		CS Driving	34
35			CS-A9		CS Driving	35

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PIN	Special Wire	Wired To	Wired To	...	Name of Signal	PIN
1		C18-11		x -	WA-6y	1
2		C18-26		x -	WA-2y	2
3		C18-33		x -	WA-4y	3
4		C18-35		x -	WA-0y	4
5		C19-11		x -	WA-7y	5
6		C19-26		x -	WA-3y	6
7		C19-33		x -	WA-5y	7
8		C19-35		x -	WA-1y	8
9		C23-26		x -	WB-7y	9
10		A19-29		x -	WY	10
11		A19-30		x -	WY	11
12		A19-8		x -	RY	12
13		A19-9		x -	RY	13
14		C23-23			RB-7y	14
15		C19-34		x -	RA-1y	15
16						16
17						17
18						18
19						19
20						20
21		C19-32		x -	RA-5y	21
22		C19-25		x -	RA-3y	22
23		C19-22		x -	RA-7y	23
24		C18-34		x -	RA-0y	24
25		C18-32		x -	RA-4y	25
26		C18-25		x -	RA-2y	26
27		C18-22		x -	RA-6y	27
28		CS-A8			CS Driving	28
29		CS-A7			CS Driving	29
30		CS-A6			CS Driving	30
31		CS-A5			CS Driving	31
32		CS-A4			CS Driving	32
33		CS-A3			CS Driving	33
34		CS-A2			CS Driving	34
35		CS-A1			CS Driving	35

Unit Buffer Store

Designed K. S. A.

Approved

Checked 1.2.63.

Last Revision

wiring schedule

Drawing No

Drawn by L. L. 15.3.69

Checked F. F. 23.10.69

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PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1				- x	WA-6x	1
2				- x	WA-2x	2
3				- x	WA-4x	3
4				- x	WA-8x	4
5				- x	WA-7x	5
6				- x	WA-3x	6
7				- x	WA-5x	7
8				- x	WA-1x	8
9		C24-35		- x	WB-Cx	9
10				- x	Wx	10
11				- x	Wx	11
12				- x	Rx	12
13				- x	Rx	13
14		C24-34		- x	RB-Qx	14
15				- x	RA-X	15
16						16
17						17
18						18
19						19
20						20
21				- x	RA-5x	21
22				- x	RA-3x	22
23				- x	RA-7x	23
24				- x	RA-Cx	24
25				- x	RA-4x	25
26				- x	RA-2x	26
27				- x	RA-6x	27
28		CS-B32			CS Driving	28
29		CS-B31			CS Driving	29
30		CS-B30			CS Driving	30
31		CS-B29			CS Driving	31
32		CS-B28			CS Driving	32
33		CS-B27			CS Driving	33
34		CS-B26			CS Driving	34
35		CS-B25			CS Driving	35


PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6x	1
2				- x -	WA-2x	2
3				- x -	WA-4x	3
4				- x -	WA-0x	4
5				- x -	WA-7x	5
6				- x -	WA-3x	6
7				- x -	WA-5x	7
8				- x -	WA-1x	8
9		C24-33		- x -	WB-4x	9
10				- x -	WX	10
11				- x -	WX	11
12				- x -	Rx	12
13				- x -	Rx	13
14		C24-32		- x -	RB-4x	14
15				- x -	RF-1x	15
16				- x -		16
17						17
18						18
19						19
20						20
21				- x -	RA-5x	21
22				- x -	RA-3x	22
23				- x -	RA-7x	23
24				- x -	RA-0x	24
25				- x -	RA-4x	25
26				- x -	RA-2x	26
27				- x -	RA-6x	27
28		CS-B24			CS Driving	28
29		CS-B23			CS Driving	29
30		CS-B22			CS Driving	30
31		CS-B21			CS Driving	31
32		CS-B20			CS Driving	32
33		CS-B19			CS Driving	33
34		CS-B18			CS Driving	34
35		CS-B17			CS Driving	35

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6x	1
2				- x -	WA-2x	2
3				- x -	WA-4x	3
4				- x -	WA-0x	4
5				- x -	WA-7x	5
6				- x -	WA-3x	6
7				- x -	WA-5x	7
8				- x -	WA-1x	8
9				- x -	WB-2x	9
10		C24-31		- x -	WA	10
11				- x -	WA	11
12				- x -	Rx	12
13				- x -	Rx	13
14				- x -	RE-2x	14
15		C24-30		- x -	RA-1x	15
16				- x -		16
17						17
18						18
19						19
20						20
21				- x -	RA-5x	21
22				- x -	RA-3x	22
23				- x -	RA-7x	23
24				- x -	WA-0x	24
25				- x -	RA-4x	25
26				- x -	WA-2x	26
27				- x -	RA-6x	27
28		CS-B16			CS Driving	28
29		CS-B15			CS Driving	29
30		CS-B14			CS Driving	30
31		CS-B13			CS Driving	31
32		CS-B12			CS Driving	32
33		CS-B11			CS Driving	33
34		CS-B10			CS Driving	34
35		CS-B9			CS Driving	35

PIN	Special Wire	Wired To	Wired To	Name of Signal	PIN
1				WA-6x	1
2				WA-2x	2
3				WA-4x	3
4				WA-5x	4
5				WA-7x	5
6				WA-3x	6
7				WA-5x	7
8				WA-1x	8
9				WB-6x	9
10				WX	10
11				WX	11
12				Rx	12
13				Rx	13
14				RB-6x	14
15				RA-1x	15
16					16
17					17
18					18
19					19
20					20
21				RA-5x	21
22				RA-3x	22
23				RA-7x	23
24				RA-0x	24
25				RA-4x	25
26				RA-2x	26
27				RA-6x	27
28				CS Driving	28
29				CS Driving	29
30				CS Driving	30
31				CS Driving	31
32				CS Driving	32
33				CS Driving	33
34				CS Driving	34
35				CS Driving	35

PIN	Special Wire	Wired To	Wired To	Name of Signal	PIN
1				WA-6x	1
2				WA-2x	2
3				WA-4x	3
4				WA-0x	4
5				WA-7x	5
6				WA-5x	6
7				WA-5x	7
8				WA-1x	8
9		C25-35		WA-1x	9
10				WA-1x	10
11				WA-1x	11
12				WA-1x	12
13				WA-1x	13
14		C25-34		WA-1x	14
15				WA-1x	15
16					16
17					17
18					18
19					19
20					20
21				WA-5x	21
22				WA-3x	22
23				WA-7x	23
24				WA-0x	24
25				WA-1x	25
26				WA-2x	26
27				WA-6x	27
28		CS-D32		CS Driving	28
29		CS-D31		CS Driving	29
30		CS-D30		CS Driving	30
31		CS-D29		CS Driving	31
32		CS-D28		CS Driving	32
33		CS-D27		CS Driving	33
34		CS-D26		CS Driving	34
35		CS-D25		CS Driving	35

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6x	1
2				- x -	WA-2x	2
3				- x -	WA-4x	3
4				- x -	WA-0x	4
5				- x -	WA-7x	5
6				- x -	WA-3x	6
7				- x -	WA-5x	7
8				- x -	WA-1x	8
9			C25-33	- x -	WB-5x	9
10				- x -	Wx	10
11				- x -	Wx	11
12				- x -	Rx	12
13				- x -	Rx	13
14			C25-32	- x -	RB-5x	14
15				- x -	RA-1x	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5x	21
22				- x -	RA-3x	22
23				- x -	RA-7x	23
24				- x -	RA-0x	24
25				- x -	RA-4x	25
26				- x -	RA-2x	26
27				- x -	RA-6x	27
28		CS-D24			CS Driving	28
29		CS-D23			CS Driving	29
30		CS-D22			CS Driving	30
31		CS-D21			CS Driving	31
32		CS-D20			CS Driving	32
33		CS-D19			CS Driving	33
34		CS-D18			CS Driving	34
35		CS-D17			CS Driving	35

	Unit: Buffer store	Designed K.H.A.
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Wiring Schedule

Drawing No	
Drawn by L.L.15.6.66.	
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C 15	1001

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1				- x -	WA-6x	1
2				- x -	WA-2x	2
3				- x -	WA-4x	3
4				- x -	WA-0x	4
5				- x -	WA-7x	5
6				- x -	WA-3x	6
7				- x -	WA-5x	7
8				- x -	WA-1x	8
9			C25-31		WB-3x	9
10				- x -	Wx	10
11				- x -	Wx	11
12				- x -	Rx	12
13				- x -	Rx	13
14			C25-30		RB-3x	14
15				- x -	RA-1x	15
16						16
17						17
18						18
19						19
20						20
21				- x -	RA-5x	21
22				- x -	RA-3x	22
23				- x -	RA-7x	23
24				- x -	RA-0x	24
25				- x -	RA-4x	25
26				- x -	RA-2x	26
27				- x -	RA-6x	27
28			CS-D16		CS Driving	28
29			CS-D15		CS Driving	29
30			CS-D14		CS Driving	30
31			CS-D13		CS Driving	31
32			CS-D12		CS Driving	32
33			CS-D11		CS Driving	33
34			CS-D10		CS Driving	34
35			CS-D9		CS Driving	35

pos. C 15 1001

Unit Buffer Store

REGNE
CENTRALEN

Designed K.H.A.

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Wiring Schedule

Drawing No

Drawn by L.L.16.3.66.

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26 Sheets

Sheet 17

C 16

1001

PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1		C20-11		x -	WA-6x	1
2		C20-26		x -	WA-2x	2
3		C20-33		x -	WA-4x	3
4		C20-35		x -	WA-0x	4
5		C21-11		x -	WA-7x	5
6		C21-26		x -	WA-3x	6
7		C21-33		x -	WA-5x	7
8		C21-35		x -	WA-1x	8
9		C25-26			WB-7x	9
10		A21-29		x -	WX	10
11		A21-30		x -	WX	11
12		A21-8		x -	Rx	12
13		A21-9		x -	Rx	13
14		C25-23			RB-7x	14
15		C21-34		x -	RA-1x	15
16						16
17						17
18						18
19						19
20						20
21		C21-32		x -	RA-5x	21
22		C21-25		x -	RA-3x	22
23		C21-22		x -	RA-7x	23
24		C20-34		x -	RA-0x	24
25		C20-32		x -	RA-4x	25
26		C20-25		x -	RA-2x	26
27		C20-22		x -	RA-6x	27
28		CS-D8			CS Driving	28
29		CS-D7			CS Driving	29
30		CS-D6			CS Driving	30
31		CS-D5			CS Driving	31
32		CS-D4			CS Driving	32
33		CS-D3			CS Driving	33
34		CS-D2			CS Driving	34
35		CS-D1			CS Driving	35

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REGNE CENTRALEN	Unit Buffer Store	Designed A.H.A.	Wiring Schedule		Drawing No		
	Approved	Checked 1.2.63.			Drawn by L.16.3.66		Sheet 11
	Last Revision	Checked F.E. 23-10-67			26 Sheets		
					C 17		

PIN	Special Wire	Wired To	Wired To	Name of Supplier	Page
1					1
2					2
3					3
4					4
5					5
6					6
7					7
8					8
9					9
10					10
11					11
12					12
13					13
14					14
15					15
16					16
17					17
18					18
19					19
20					20
21					21
22					22
23					23
24					24
25					25
26					26
27					27
28					28
29					29
30					30
31					31
32					32
33					33
34					34
35					35

pos. C 17

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1		F14-29		- x	AD 1	1
2		F14-24		- x	AD 1	2
3		F13-29		- x	AD 0	3
4		F13-24		- x	AD 0	4
5		F15-29		- x	AD 2	5
6	- 8 Volts	C18-8		- x	- 8 Volts	6
7						7
8	- 8 Volts	C18-6		- x	- 8 Volts	8
9	- 8 Volts	B18-9		- x	- 8 Volts	9
10	- 1.6 Volts	A19-15		- x	- 1.6 Volts	10
11		C8-1			WA 6v	11
12						12
13				- x	Wt	13
14				- x	Rt	14
15	0 Volts			- x	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts	C18-30		- x	0 Volts	21
22		C8-27			RA 6v	22
23						23
24						24
25		C8-26			RA 2v	25
26		C8-2			WA 2v	26
27	- 24 Volts			- x	- 24 Volts	27
28	+ 8 Volts	B18-8		- x	+ 8 Volts	28
29	+ 24 Volts			- x	+ 24 Volts	29
30	0 Volts	C18-21		- x	0 Volts	30
31	- 3.2 Volts	A19-27		- x	- 3.2 Volts	31
32		C8-25			RA 4v	32
33		C8-3			WA 4v	33
34		C8-24			RA 0v	34
35		C8-4			WA 0v	35

Designed **K.H.A.**

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Wiring Schedule

Drawing No

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26 Sheets

Sheet **20**

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1003-2

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1				x -	AD 1	1
2				x -	AD 1	2
3				x -	AD 0	3
4				x -	AD 0	4
5					AD 2	5
6	- 8 Volts	F15-24		- x -	- 8 volts	6
7						7
8	- 8 Volts			- x -	- 8 Volts	8
9	- 8 Volts			- x -	- 8 Volts	9
10	- 1.6 Volts			- x -	- 1.6 Volts	10
11		Cu-5			WA 7y	11
12						12
13				- x -	Rt	13
14				- x -	Rt	14
15	0 Volts			- x -	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x -	0 Volts	21
22		C8-23			RA 7y	22
23						23
24						24
25		C8-22			RA 3y	25
26		C8-6			WA 3y	26
27	- 24 Volts			- x -	- 24 Volts	27
28	+ 8 Volts			- x -	+ 8 Volts	28
29	+ 24 Volts			- x -	+ 24 Volts	29
30	0 Volts			- x -	0 Volts	30
31	- 3.2 Volts			- x -	- 3.2 Volts	31
32		C8-21			RA 5y	32
33		C8-7			WA 5y	33
34		C8-15			RA 1y	34
35		C8-8			WA 1y	35

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1		F18-29		-x-	AD 4	1
2		F18-24		-x-	AD 4	2
3		F16-29		-x-	AD 3	3
4		F16-24		-x-	AD 3	4
5		F19-29		-x-	AD 5	5
6	- 8 Volts			-x-	- 8 Volts	6
7						7
8	- 8 Volts			-x-	- 8 Volts	8
9	- 8 Volts			-x-	- 8 Volts	9
10	- 1.6 Volts			-x-	- 1.6 Volts	10
11		C16-1			RA 6x	11
12						12
13				-x-	wt	13
14				-x-	Rt	14
15	0 Volts			-x-	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			-x-	0 Volts	21
22		C16-27			RA 6x	22
23						23
24						24
25		C16-26			RA 2x	25
26		C16-2			WA 2x	26
27	- 24 Volts	B20-12		-x-	- 24 Volts	27
28	+ 8 Volts			-x-	+ 8 Volts	28
29	+ 24 Volts			-x-	+ 24 Volts	29
30	0 Volts			-x-	0 Volts	30
31	- 3.2 Volts			-x-	- 3.2 Volts	31
32		C16-25			RA 4x	32
33		C16-3			WA 4x	33
34		C16-24			RA 0x	34
35		C16-4			WA 0x	35

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1				x -	AD 4	1
2				x -	AD 4	2
3				x -	AD 3	3
4				x -	AD 3	4
5					AD 5	5
6	- 8 Volts		F19-24	- x -	- 6 Volts	6
7						7
8	- 8 Volts			x -	- 8 Volts	8
9	- 8 Volts			x -	- 8 Volts	9
10	- 1.6 Volts			- x -	- 1.6 Volts	10
11					WA 7x	11
12						12
13				x -	Wt	13
14				x -	Rt	14
15	0 Volts			- x -	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x -	0 Volts	21
22					RA 7x	22
23						23
24						24
25					RA 3x	25
26					WA 3x	26
27	- 24 Volts			- x -	- 24 Volts	27
28	+ 8 Volts			x -	+ 8 Volts	28
29	+ 24 Volts			- x -	+ 24 Volts	29
30	0 Volts			x -	0 Volts	30
31	- 3.2 Volts			x -	- 3.2 Volts	31
32					RA 5x	32
33					WA 5x	33
34					RA 1x	34
35					WA 1x	35

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1		F21-29		-x-	AD 7	1
2		F21-24		-x-	AD 7	2
3		F20-29		-x-	AD 6	3
4		F20-24		-x-	AD 6	4
5		F22-29		-x-	AD 6	5
6	- 8 Volts			-x-	- 8 Volts	6
7						7
8						8
9						9
10	- 1.6 Volts			-x-	- 1.6 Volts	10
11						11
12	- 8 Volts			-x-	- 8 Volts	12
13		C21-14		-x-	Rt	13
14		C21-13		-x-	Wt	14
15	0 Volts			-x-	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			-x-	0 Volts	21
22						22
23		C4-14			RE 6v	23
24	- 8 Volts			-x-	- 8 Volts	24
25	- 8 Volts			-x-	- 8 Volts	25
26		C4-9			WB 6v	26
27	- 24 Volts			-x-	- 24 Volts	27
28	- 8 Volts			-x-	- 8 Volts	28
29	+ 24 Volts	A22-1		-x-	+ 24 Volts	29
30		C3-14			RB 2v	30
31		C3-9			WB 2v	31
32		C2-14			RB 4v	32
33		C2-9			WB 4v	33
34		C1-14			RB 4v	34
35		C1-9			WB 0v	35

PIN	Special Wire	Wired To	Wired To	--x--	Name of Signal	PIN
1				x -	AD 7	1
2				x -	AD 7	2
3				x -	AD 6	3
4				x -	AD 6	4
5					AD 6	5
6	- 8 Volts	F22-24		- x -	- 8 Volts	6
7						7
8						8
9						9
10	- 1.6 Volts			- x -	- 1.6 Volts	10
11						11
12	- 8 Volts			- x -	8 Volts	12
13				- x -	Pt	13
14				- x -	Wt	14
15	0 Volts			- x -	0 Volts	15
16						16
17						17
18						18
19						19
20						20
21	0 Volts			- x -	0 Volts	21
22						22
23		C8-14			RE 7	23
24	- 8 Volts			- x -	- 8 Volts	24
25	- 8 Volts			- x -	- 8 Volts	25
26		C8-9			WE 7y	26
27	- 24 Volts			- x -	- 24 Volts	27
28	- 8 Volts			- x -	- 8 Volts	28
29	+ 24 Volts			- x -	+ 24 Volts	29
30		C7-14			RE 3y	30
31		CY-9			WE 3y	31
32		C6-14			RE 5y	32
33		C6-9			WE 5y	33
34		C5-14			RE 1y	34
35		C5-9			WE 1y	35

PIN	Special Wire	Wired To	Wired To	- x -	Name of Signal	PIN
1		F24-27		- x	AE 13	1
2		F24-24		- x	AE 12	2
3		F23-29		- x	AE 11	3
4		F23-24		- x	AE 10	4
5		F25-27		- x	AE 11	5
6	- 8 Volts			- x	- 8 Volts	6
7						7
8						8
9						9
10	- 1.6 Volts	B24-4		- x	- 1.6 Volts	10
11						11
12	- 8 Volts			- x	- 8 Volts	12
13				- x	Rt	13
14				- x	Wt	14
15	0 Volts			- x	0 Volts	15
16				- x		16
17						17
18						18
19						19
20						20
21	0 Volts			- x	0 Volts	21
22						22
23		C12-14			RE 6x	23
24	- 8 Volts			- x	- 8 Volts	24
25	- 8 Volts			- x	- 8 Volts	25
26		C12-7			WB 6x	26
27	- 24 Volts			- x	- 24 Volts	27
28	- 8 Volts			- x	- 8 Volts	28
29	+ 24 Volts			- x	+ 24 Volts	29
30		C11-14			RB 2x	30
31		C11-9			WB 2x	31
32		C13-14			RB 4x	32
33		C10-9			WB 4x	33
34		C7-14			RB 1x	34
35		C9-9			RB 0x	35

PIN	Special Wire	Wired To	Wired To	-x-	Name of Signal	PIN
1				x -	AB 1x	1
2				x -	AB 2x	2
3				x -	AB 3x	3
4				x -	AB 4x	4
5		F25-24			AB 5x	5
6	- 8 Volts	- 8 V Term. P.S.		x -	AB 6x	6
7					AB 7x	7
8					AB 8x	8
9					AB 9x	9
10	- 1.6 Volts	- 1.6 V Term. P.S.		x -	AB 10x	10
11					AB 11x	11
12	- 3 Volts	- 3 V Term. P.S.		x -	AB 12x	12
13		B23-1		x -	AB 13x	13
14		B23-3		x -	AB 14x	14
15	0 Volts			x -	AB 15x	15
16					AB 16x	16
17					AB 17x	17
18					AB 18x	18
19					AB 19x	19
20					AB 20x	20
21	0 Volts			x -	AB 21x	21
22					AB 22x	22
23		C16-14			AB 23x	23
24	- 8 Volts	- 8 V Term. P.S.		x -	AB 24x	24
25	- 8 Volts	- 8 V Term. P.S.		x -	AB 25x	25
26		C16-9			AB 26x	26
27	- 24 Volts	- 24 V Term. P.S.		x -	AB 27x	27
28	- 8 Volts	- 8 V Term. P.S.		x -	AB 28x	28
29	+ 24 Volts	+ 24 V Term. P.S.		x -	AB 29x	29
30		C16-14			AB 30x	30
31		C15-9			AB 31x	31
32		C14-14			AB 32x	32
33		C14-9			AB 33x	33
34		C13-14			AB 34x	34
35		C13-9			AB 35x	35